MAINTENANCE MANUAL

FDS-100 MINIFILE

G.U.C. PRODUCTS
Santee, California

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1.0 GENERAL DESCRIPTION

The FDS-100 Minifile is a self-contained minifloppy disk drive, controller and power supply in a rugged metal enclosure. Figure 1 is a system block diagram of the FDS-100.

The controller is comprised of three printed circuit cards; Control Card, Disk Interface Card, and Serial Interface Card. These cards plug into three card edge connectors mounted on the printed circuit backplane and interconnected by means of a BUS. Connector positions are not dedicated and it is functionally irrelevant which card plugs into which connector.

The Status LED indicators are the three LED's on the front panel which display the current FDS-100 status. They are ACTIVITY, STATUS, and FILE OPEN.

The Control Card contains a microprocessor, up to 6K bytes of EPROM, 1K byte of RAM and some additional circuitry for generating clocks and handling interrupts. The system firmware, stored in the EPROM, establishes the functional characteristics of the FDS-100. Driven by the firmware program, the Control Card monitors and controls the Disk Interface and Serial Interface cards. RAM is for program variables and buffer space for data transfers to and from the HOST device. RAM is also used for file management functions.

The Disk Interface contains the necessary circuitry to control, read, and write the floppy disk drive. This card provides drive status information to the control card when requested by the firmware. Data are transferred via direct memory access (DMA) to and from the RAM located on the Control Card.

The Serial Interface Card provides the interface between the HOST device and the FDS-100 via an RS-232C port. This card contains the circuitry required to assemble and disassemble 8 bit characters across the RS-232C lines. Interrupts are generated for the Control Card when characters are transmitted or received. Two DIP switches are also on this card to allow selection of various options such as baud rate, parity, stop bits, and block check.

The Floppy Disk Drive shown in Figure 1 is a Shugart SA400 minifloppy disk drive or equivalent. This drive uses 5.25 inch diskettes as the storage medium.

The Power Supply is an integral part of the unit and is of the switching power supply variety. It provides DC power to all the controller boards and to the drive. Three voltages are used: +5 VDC, +12 VDC, and -12 VDC.

The dashed lines in Figure 1 (keyboard and display) shown are applicable only to the Model SK. A twelve key numeric keyboard and three seven-segment display LED's are mounted on the front panel. They are used by the operator to enter file management commands and to display operational status of the FDS-100 SK to the operator.

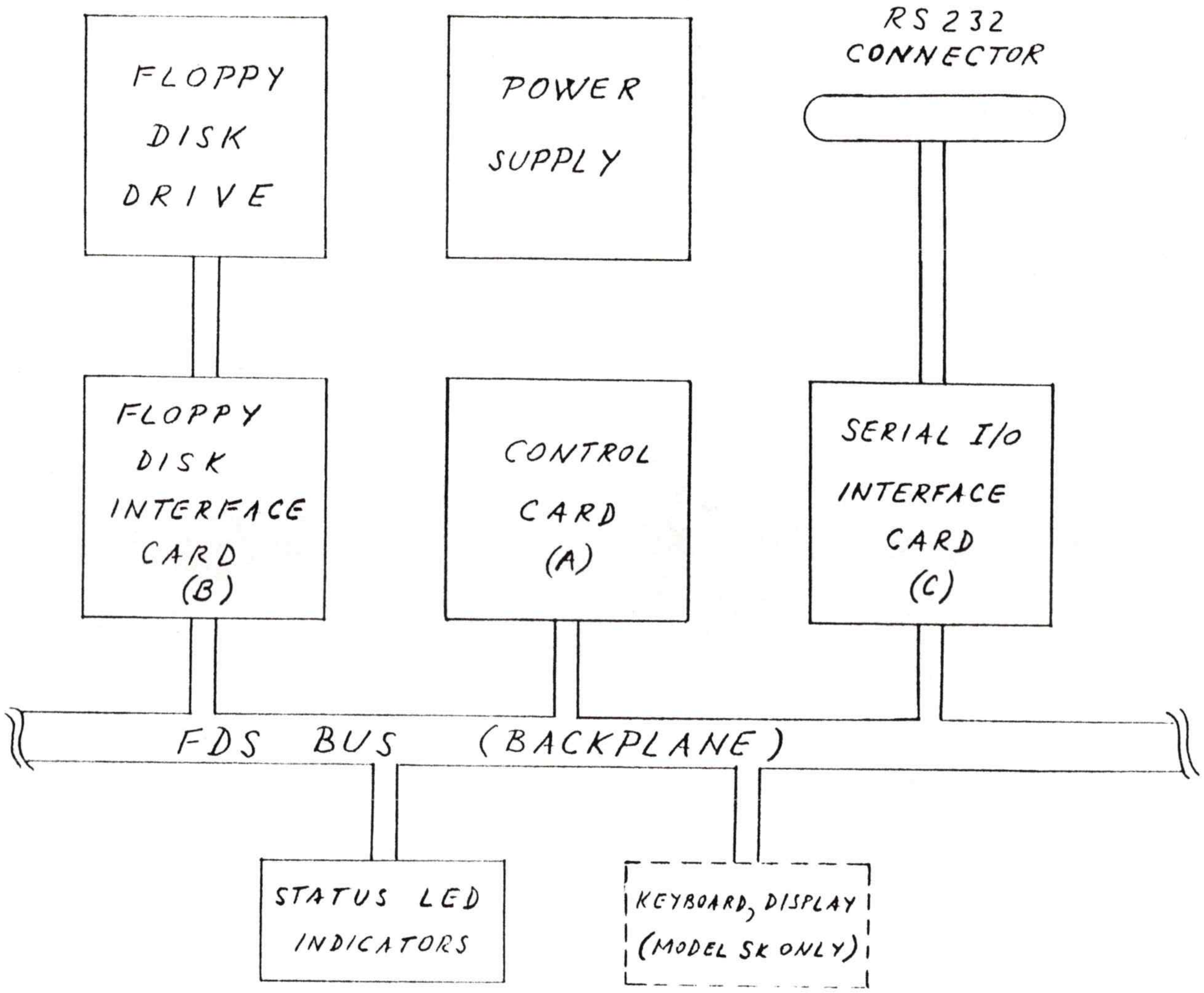

FIG. 1. FDS-100 FUNCTIONAL BLOCK DIAGRAM

1.1 BUS AND BACKPLANE

The controller, made up of the three cards described in section 1.0 is interconnected by means of a BUS. This BUS is a set of Data, Address, and Control signals as listed in Table 1. The Backplane is a physical implementation of the BUS. It is a printed circuit board that provides connections between the three card edge connectors it carries. A power up initialize circuit is also provided on the Backplane. See sheet 4 of drawing 10221 in Appendix A.

J1	J2	J3	SIGNAL
1	1	1	COM
2	2	2	COM
3	3	3	COM
4	4	4	COM
5	5	5	+5 VDC
6	6	6	+5 VDC
7	7	7	+5 VDC
8	8	8	+5 VDC
9	9	9	-5 VDC
10	10	10	-5 VDC
11	11	11	-12 VDC
12	12	12	-12 VDC
13	13	13	+12 VDC
14	14	14	+12 VDC
15	15	15	COM
16	16	16	COM
17	17	17	ADR001
18	18	18	ADR011
19	19	19	ADR021
20	20	20	ADR031
21	21	21	ADR041
22	22	22	ADR051
23	23	23	ADR061
24	24	24	ADR071
25	25	25	ADR081
26	26	26	ADR091
27	27	27	ADR010
28	28	28	ADR011
29	29	29	ADR012
30	30	30	ADR013
31	31	31	ADR014
32	32	32	DBUS01
33	33	33	DBUS11
34	34	34	DBUS21
35	35	35	DBUS31
36	36	36	DBUS41
37	37	37	DBUS51
38	38	38	DBUS61
39	39	39	DBUS71
40	40	40	INTR00
41	41	41	LACT0
42	42	42	INTR10
43	43	43	LSTS0
44	44	44	INTR20
45	45	45	LOPN0
46	46	46	INTR30
47	47	47	COM
48	48	48	IOS0
49	49	49	COM
50	50	50	OPREQ0
51	51	51	COM
52	52	52	ROW1
53	53	53	COM
54	54	54	RESET0
55	55	55	BACKI0
56	56	56	BACKO0
57	57	57	COM
58	58	58	CLOCK0
59	59	59	INTAKI0
60	60	60	INTAKO0
61	61	61	COM
62	62	62	WRP0
63	63	63	COM
64	64	64	M1IO0
65	65	65	COM
66	66	66	BREQ0
67	67	67	COM
68	68	68	PURST0
69	69	69	COM
70	70	70	OPACK1
71	71	71	COM
72	72	72	INTREQ0
73	73	73	+5 VDC
74	74	74	+5 VDC
75	75	75	+5 VDC
76	76	76	+5 VDC
77	77	77	COM
78	78	78	COM
79	79	79	COM
80	80	80	COM

TABLE 1

1.2 CONTROL CARD

Figure 2 is a block diagram of the Control Card. Schematic drawings for the Control Card are located in Appendix A of this manual. (reference drawing 10161)

The central elements of the Control Card are the microprocessor, EPROM, RAM, Clock Generator, 3-State Receivers and Drivers, and the Interrupt Priority Arbitration logic.

The micropre̤cessor is a Signetics 2650. Reference sheet 1 of schematic. All outputs of the 2650 are buffered with 3-State drivers, and bi-directional signals are isolated with 3-State receivers. The 2650 utilizes a 1 MHZ clock supplied by the Clock Generator (CLOCK1). This clock is also present on the backplane. The microprecessor instructions take between 6 and 12 clock cycles for completion.

The microprocessor fetches instructions from the EPROM located on this card (sheet 2 of schematic). Program variables and data buffers are maintained in RAM (sheet 3 of schematic). Address mapping for memory (EPROM, RAM) is assigned as follows:

ADDRESS RANGE	2708 EPROM	2716 EPROM	RAM
0000-03FF	U1	U1	-
0400-07FF	U2	U1	-
0800-0BFF	U3	U2	-
0C00-0FFF	U9	U2	-
1000-13FF	U10*	-	-
1400-17FF	U11*	-	-
1800-1BFF	-	-	U5, U7*
1C00-1FFF	-	-	U4, U6

*not installed

1.2.1 CLOCK GENERATOR

The Control Card contains a 2.00 MHZ crystal clock oscillator (sheet 5 of schematic). The 2 MHZ clock is divided down to provide the 1 MHZ system clock (CLOCK1). This clock is also supplied to the backplane for other cards in the system. The clock is further divided down to provide program interrupts at 8 millisecond intervals (sheet 4 of schematic). These interrupts are used by the firmware to drive scheduled events which are queued to take place at some multiple of that interval. For example, the allotted time for the floppy drive motor to remain ON without reading or writing is 30 seconds. This 30 second time is re-established each time a read or write operation takes place. If this time should expire, the drive motor is turned OFF. Other scheduled events or timed operations are as follows:

a) Motor up to speed	1 second
b) Head load settling time	80 milliseconds
c) Head step time	48 milliseconds
d) Max head load time without access	2 seconds

1.2.2 INTERRUPTS

The 2650 microprocessor supports a vectored interrupt scheme. The handshaking for this scheme is local to the Control Card (sheet 4 of schematic). The schematic shows a priority encoder (74LS148) of which its outputs are taken to a data bus driver to supply the address vector. The inputs to the priority encoder are assigned to individual cards in the system. The card switches its line low to cause a program interrupt. Interrupts assignments are as follows:

PRIORITY	VECTOR	DESCRIPTION
INTR00 (highest)	04	Serial Interface
INTR10	06	Disk Interface
INTR20	08	Not Used
INTR30	0A	Not Used
INTR40	0C	Program Clock

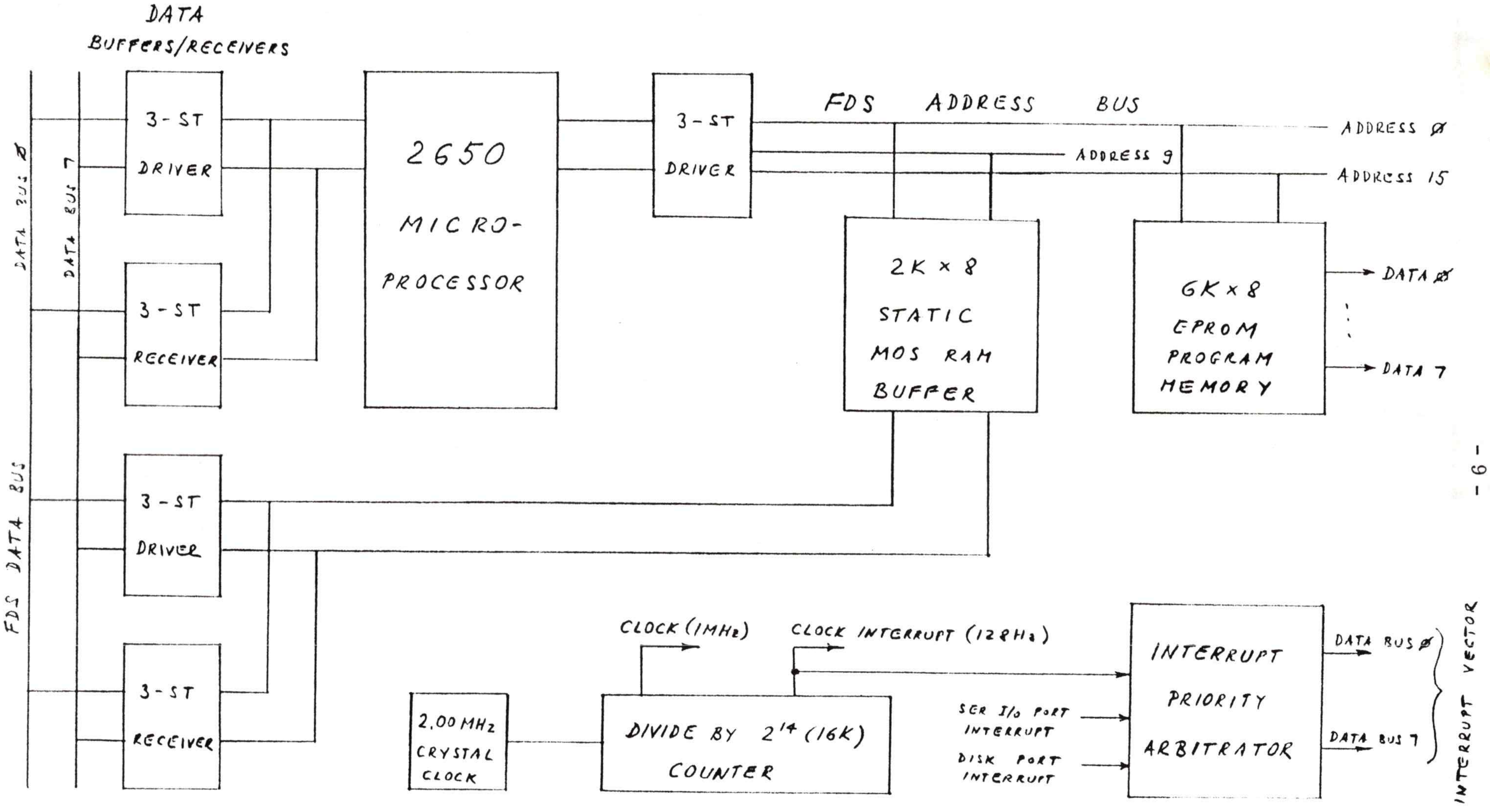

FIG. 2: CONTROL CARD BLOCK DIAGRAM

1.3 DISK INTERFACE CARD

Figure 3 is a block diagram of the Disk Interface Card. Schematic drawings for the Disk Interface Card are located in Appendix A of this manual. (reference drawing 10171)

The BYTE COUNTER AND MEMORY ADDRESS GENERATOR section (sheet 1 of schematic) performs a twofold function. The counter counts the number of bytes transferred between the floppy disk and the buffer memory (sheet 3, drawing 10161). The counter is initialized to the negative equivalent of the number of bytes to be transferred. The transfer is performed under control of the DMA control logic (sheet 1 of schematic), which increments the counter by one for each byte transferred. The counter output, buffered thru 3-State buffers, provides the memory address for each byte. Counter overflow stops the transfer by setting WCOF true (word count overflow).

This controller uses hard sectored floppy diskettes in which timing pulses (SECTOR0) are generated by a sensor in the drive which is sensing physical holes in the diskette. They are fed into the SECTOR MARK AND ORIGIN PULSE DISCRIMINATOR circuitry (sheet 2 of schematic) which generates sector mark pulses (SM0) and origin pulses (OP0). OP0 is then used to clear the SECTOR COUNTER (sheet 2 of schematic) while SM0 is used to increment it. The contents of this sector counter along with two other status signals provided by the floppy drive are available to the microprocessor. The two signals are TRACK ZERO (TRK00) and WRITE PROTECT (WPROT0).

The DISK CONTROL REGISTER (sheet 2 of schematic) can be loaded by the microprocessor to provide control signals necessary for the disk drive operation. The signals are as follows:

BIT	SIGNAL	DESCRIPTION
DBUS21 (2)	DIR0	HEAD STEP DIRECTION
DBUS31 (3)	STEP0	HEAD STEP
DBUS41 (4)	MOTOR0	MOTOR ON
DBUS41 (5)	DS10	DRIVE SELECT 1
DBUS61 (6)	DS20	DRIVE SELECT 2 (Not Used)
DBUS71 (7)	SIDE20	SIDE 2 (Not Used)

The READ CLOCK GENERATOR circuit (sheet 3 of schematic) generates the DISK READ CLOCK signal (RDCLK0) from DISK READ DATA (RDATA0). The DISK READ CLOCK signal is then fed to the READ/WRITE CLOCK GENERATOR circuit (sheet 2 of schematic) which generates BYTE CLOCK and BIT CLOCK signals during a read operation.

The PARALLEL TO SERIAL AND SERIAL TO PARALLEL CONVERTOR circuitry is shown on sheet 3 of the schematic. This is a pair of shift registers-buffers that is used to form the serial stream of disk data in a disk read operation into bytes suitable for storing into the RAM buffer memory. For a disk write operation it takes bytes of data from the RAM buffer and converts them into a serial stream of bits for disk storage.

During a disk read operation RDCLK0 and RDATA0 signals are fed into the READ DATA DECODER (sheet 3 of schematic). This decoder converts phase modulated data from the diskette into NRZ. Decoded data are fed into the serial input of the shift register and shifted in by means of clock INCLK0. After an entire byte has been shifted into the shift register (4A and 5A on sheet 3 of schematic), a byte parallel transfer is performed into shift register (4B and 5B). From there the byte is transferred into the RAM memory buffer via DMA.

During a disk write operation, a byte of data is parallel loaded into the 4A-5A shift register-buffer and then transferred into the second register pair (4B and 5B). Then by means of clock pulses OCK0 this byte is shifted out, bit by bit, from the 4B-5B register into the WRITE DATA ENCODER (sheet 3 of schematic). Binary data are converted into phase modulated write data suitable for writing on the diskette.

The recorded data on each sector of a diskette is broken up into several sections as follows:

SEQUENCE	SECTION	NUMBER OF BYTES
1	PREAMBLE	15
2	DATA HEADER	2
3	DATA	160
4	CHECK	2
5	POSTAMBLE	2

1.3.1 DISK INTERFACE ALIGNMENT

Three trim POTS are provided on this circuit card (R3, R5, R11). R11 is adjusted to obtain proper separation of the OP0 and SM0 timing pulses. R3 is set to ensure synchronization to the recorded data to begin in the center of the recorded preamble. R5 is adjusted for optimum data recovery. The procedure for making the above adjustments requires a pre-recorded diskette and an oscilloscope. With the diskette installed and power applied, ground signals MOTOR0 and DS10. Make each adjustment in the order shown below:

TRIM POT	MONITOR	TRIGGER	TIME
R11	1D-4	NEG	10 ms
R3	4E-4	NEG	500 us
R5	4E-12	NEG	6.1 us

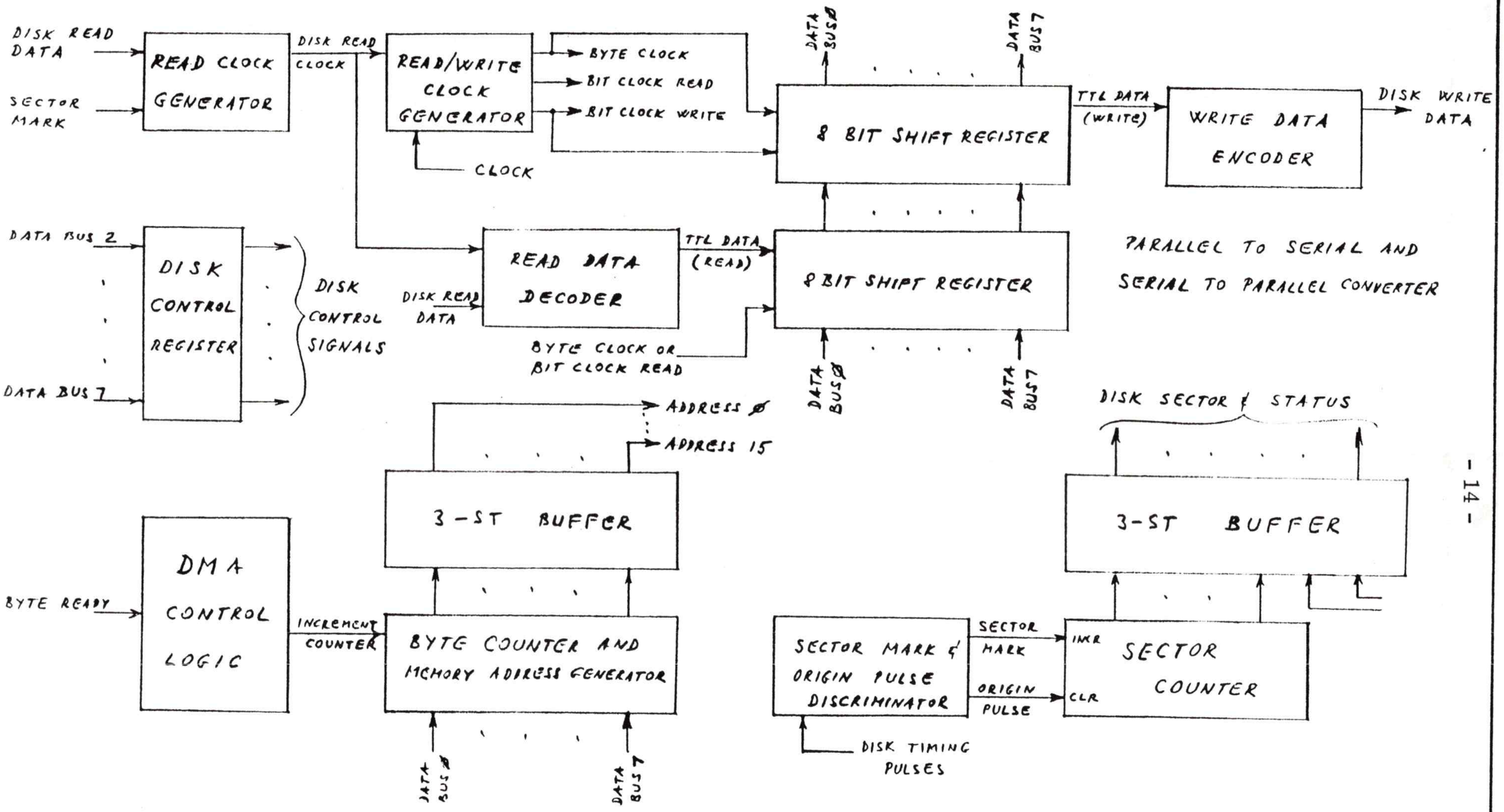

FIG. 3 : FLOPPY DISK INTERFACE CARD

1.4 SERIAL INTERFACE CARD

Figure 4 is a block diagram of the Serial Interface Card. Schematic drawings for the Serial Interface Card are located in appendix A of this manual. (reference drawing 10181) Rear panel I/O connector pin assignments are shown in appendix A. (reference drawing 20241)

The Serial Interface utilizes a PROGRAMMABLE USART (sheet 1 of schematic, Universal Synchronous Asynchronous Receiver Transmitter). Internally, the USART converts parallel 8 bit data bytes to serial data and adds start and stop bits for transmission. In the reverse direction, the USART strips off the start and stop bits and converts the 8 bit serial data to a parallel 8 bit byte. Parameters (i.e., stop bits, baud rate, etc.) are contained in control registers internal to the USART and set up by the microprocessor located on the Control Card. For each character transmitted or received, an interrupt is generated to the Contol Card (INTR00).

The 8 bit parallel path (D0-D7) provided by the USART is a bi-directional bus. This path is further buffered with Data Buffer/Receivers onto the BUS. The serial input and output of the USART are of TTL levels. These levels are converted to and from RS-232C levels with RS-232C Receivers and Drivers (sheet 3 of schematic).

The USART requires a 5.0688 MHZ clock. A crystal oscillator at the required frequency is contained on this card (sheet 1 of schematic).

There are two sets of 8 contact DIP switches on this card which are used to establish the operating parameters of the Serial Interface (sheet 2 of schematic). Settings for these switches are published in the Operators Manual. The switch positions are read by the microprocessor in two 8 bit bytes and decoded by the firmware.

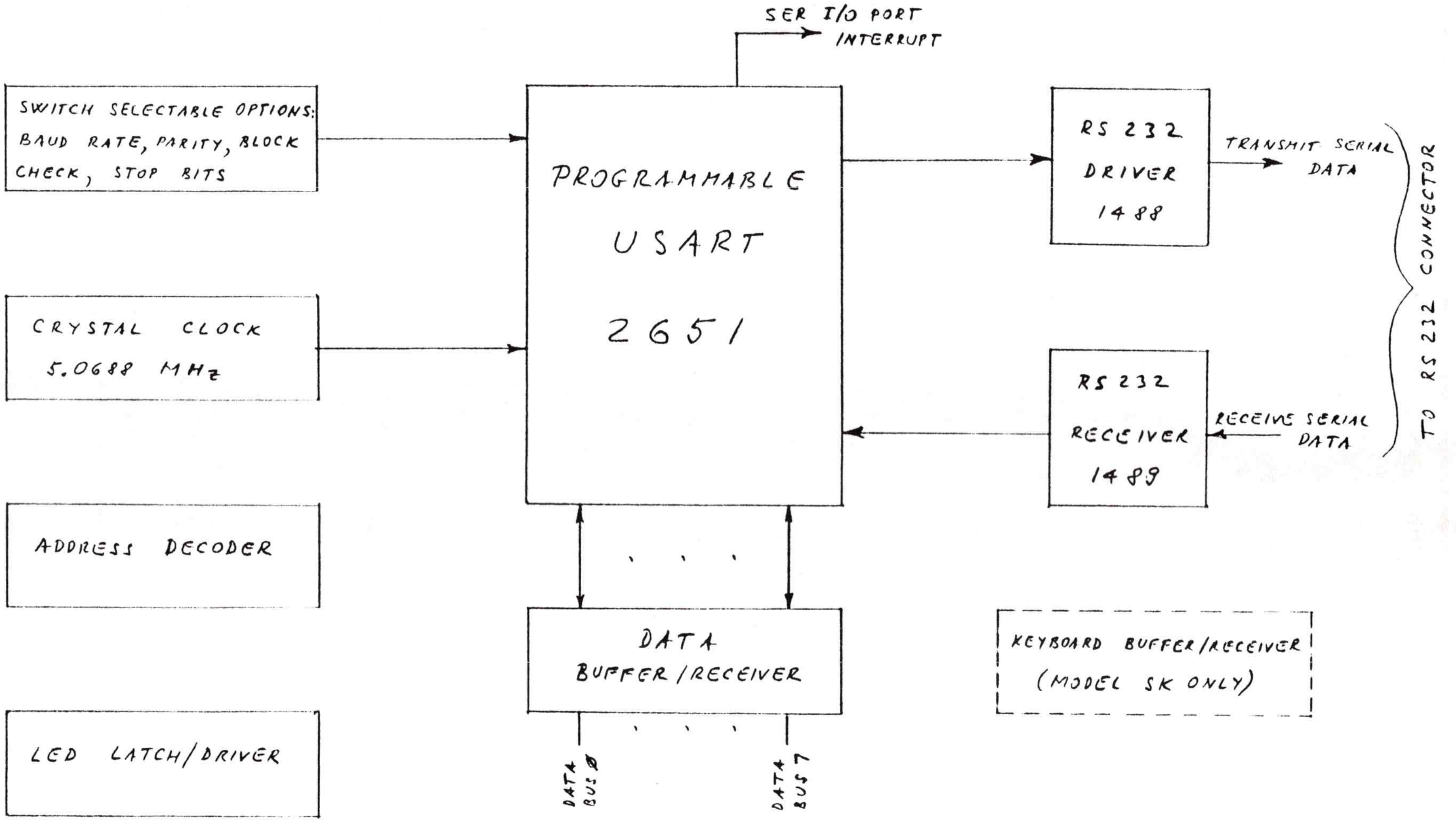

FIG 4.: SERIAL I/O INTERFACE CARD

1.5 POWER DISTRIBUTION

The Power Distribution schematic diagram is shown in Appendix A of this manual (reference drawing 10231).

The FDS-100 is a self-contained unit with a DC power supply which operates off 115 VAC nominal 50HZ to 60HZ. AC power is switched by S1 which is physically located at the rear of the unit. A fuse (F1) is provided in series with the high side of the AC line and is physically located on the inside of the rear panel. Replacement of this fuse should be of exact size and type (AGC 1).

There are three DC voltage outputs of the power supply. These outputs are connected directly to the Backplane printed circuit card and in turn supplied to the controller cards and floppy disk drive.

APPENDIX

LIST OF DRAWINGS

DRAWING TITLE	DRAWING NUMBER
FDS-100S Top Assembly	RS232C-SD
Backplane Assembly	10220
Backplane Schematic	10221
Control Circuit Card Assembly	10160
Control Circuit Card Schematic	10161
Disk Interface Card Assembly	10170
Disk Interface Card Schematic	10171
Disk I/O Harness Schematic	20231
Serial I/O Card Assembly	10180
Serial I/O Card Schematic	10181
Serial I/O Harness Schematic	20241
Rear Panel Assembly	10060
Power Distribution Schematic	10231

FDS-100S P/N RS232C-SD

QTY	PART NUMBER	DESCRIPTION	VENDOR
1	20110-1	DRIVE MNTG BRKT/CARD CAGE	
1	20110-2	DRIVE MNTG BRKT/CARD CAGE	
1	20120	FRONT PANEL	
1	10060	REAR PANEL ASSEMBLY	
1	20160	TOP COVER	
1	20170	BOTTOM COVER	
1	SA400	MINIFLOPPY DRIVE	SHUGART *
1	AC92219	POWER SUPPLY	ASTEC *
1	10160	CONTROL CIRCUIT CARD	
1	40020-1	IC, PROM	
1	40020-2	IC, PROM	
1	10170	DISK INTERFACE CIRCUIT CARD	
1	10180	SERIAL I/O CIRCUIT CARD	
6	I-650	CARD GUIDE	BIVAR
1	E1015-07.5 BLK	POWER CORD	ELECTRO CORD *
1	504-4405	FUSE BLOCK	HOUSER
1	AGC-1	1 AMP FUSE	
4	505-F63	RUBBER FEET	
4	8248	1/4 INCH STANDOFF	SMITH
1	2093	HANDLE	SMITH
4		8-32X5/8 SCREWS,PHILLIPS,FLAT	
4		8-32X1/2 SCREWS, PHILLIPS, FLAT HEAD, 100 DEG.	
1	20290	SCREEN, BOTTOM COVER AIR VENT	
A/R	SC-42	1/8X1/2 SPONGE TAPE	ROYAL IND.
4		6-32X1/8 PAN HD PHLPS SCREW	
7		6-32X3/8 PAN HD PHLPS SCREW	
1		6-32 NUT	
7		#6 FLAT WASHER	
4		6-32-1/2 PAN HD PHLPS SCREW	
10		1/8X1/8 POP RIVET	
6		4-40X3/8 PAN HD PHLPS SCREW	
2		4-40X1/2 PAN HD PHLPS SCREW	
2		4-40 NUT	
12		#4 FLAT WASHER	
2		#4 INTERNAL TOOTH LOCK WASHER	
4		#6, 1/4 IN. SPACER	
A/R	528-MP-A	MNTG PLTFRM, ADHESIVE BACK	HOUSER *
A/R	528-NT-70	NYLON TIE	HOUSER *
1	20230	HARNESS, DISK INTERFACE	
2	20270	SPACER	
A/R		BRN 16 GA. STRANDED WIRE	
A/R		BLK 20 GA. STRANDED WIRE	
A/R		LOCTITE	

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APPROVAL	DATE			
	6/79	FDS-100S TOP ASSEMBLY		
	6/79	DRAWING	REV	DATE
		RS232C-SD	A	
		SHEET: 1	OF 1	

FDS-100 ASSY

FDS-100S BACKPLANE ASSEMBLY P/N 10220

QTY	PART NUMBER	DESCRIPTION	VENDOR	REF. DESIGNATOR
1	10223	P.C. BOARD		
3	3KH40/9CND3	80 PIN EDGE CONNECTOR	VIKING *	J1,J2,J3
3	579-229R	LED, RED	HOUSER	L1,L2,L3
1	2N2907A	TRANSISTOR		Q2
1	2N2222A	TRANSISTOR		Q1
1	1N914A	DIODE		D1
1		750 OHM, 1/4 W RES.		R5
2		5.1K OHM, 1/4 W RES		R3,R4
1		10K OHM, 1/4 W RES		R2
1		51K OHM, 1/4 W RES.		R1
1	T110B685K035AS	6.8 MF., 35V CAP.	KEMET *	C1
1	CK06BX104K	.1 MF. CAP.		C2
4		16 GA., #6 RING TERMINALS		
3	60619-1	CRIMP SOCKETS	AMP *	
1	1-480424-0	HOUSING	AMP *	
A/R		BLK 16 GA. STRANDED WIRE		
A/R		BRN 16 GA. STRANDED WIRE		
A/R		RED 16 GA. STRANDED WIRE		
A/R		WHT 16 GA. STRANDED WIRE		
REF	10221	SCHEMATIC		

* OR EQUIVALENT

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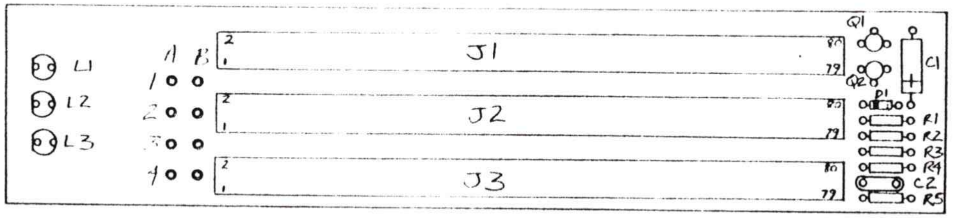
APPROVAL	DATE	BACKPLANE ASSEMBLY		
	5/79	DRAWING	REV	DATE
	5/79	10220	A	
		SHEET: 1 OF 2		

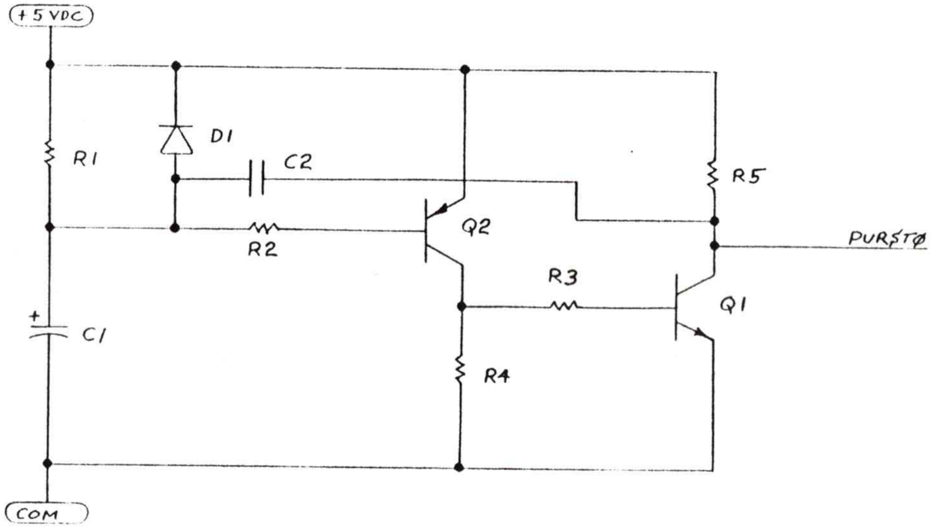


	COLOR/GAUGE	LENGTH	TERMINATION
1A	NONE		
2A	WHT/16	22.0"	AMP 60619-1 PIN 1 IN AMP 1-480424-0 HOUSING
3A	BRN/16	22.0"	AMP 60619-1 PIN 4
4A	BLK/16	22.0"	AMP 60619-1 PIN 2
1B	RED/16	4.0"	16 GA, #6 RING TERMINAL -12 VDC
2B	WHT/16	5.5"	16 GA, #6 RING TERMINAL +12VDC
3B	BRN/16	4.5"	16 GA, #6 RING TERMINAL +5VDC
4B	BLK/16	4.0"	16 GA, #6 RING TERMINAL COM

CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	ASSEMBLY DRAWING, BACKPLANE
DRAWN KWG	5/79	
CHECKED	6/79	

SIZE | CODE IDENT NO. | DRAWING NO. 10220 REV A

SCALE | SHEET 2 OF 2



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	
DRAWN	6/79	SCHEMATIC, BACKPLANE
CHECKED	6/79	

SIZE	CODE IDENT NO.	DRAWING NO.
		10221B

SCALE

SHEET 1 OF 2

J1	J2	J3	SIGNAL
1	1	1	COM
2	2	2	COM
3	3	3	COM
4	4	4	COM
5	5	5	+5 VDC
6	6	6	+5 VDC
7	7	7	+5 VDC
8	8	8	+5 VDC
9	9	9	-5 VDC
10	10	10	-5 VDC
11	11	11	-12 VDC
12	12	12	-12 VDC
13	13	13	+12 VDC
14	14	14	+12 VDC
15	15	15	COM
16	16	16	COM
17	17	17	ADR001
18	18	18	ADR011
19	19	19	ADR021
20	20	20	ADR031
21	21	21	ADR041
22	22	22	ADR051
23	23	23	ADR061
24	24	24	ADR071
25	25	25	ADR081
26	26	26	ADR091
27	27	27	ADR010
28	28	28	ADR011
29	29	29	ADR012
30	30	30	ADR013
31	31	31	ADR014
32	32	32	DBUS01
33	33	33	DBUS11
34	34	34	DBUS21
35	35	35	DBUS31
36	36	36	DBUS41
37	37	37	DBUS51
38	38	38	DBUS61
39	39	39	DBUS71
40	40	40	INTR00

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APPROVAL	DATE	BACKPLANE		
	5/25/79	DRAWING	REV	DATE
	5/25/79	10221	B	
		SHEET: 2 OF 3		

J1	J2	J3	SIGNAL
41	41	41	LACT0
42	42	42	INTR10
43	43	43	LSTS0
44	44	44	INTR20
45	45	45	LOPN0
46	46	46	INTR30
47	47	47	COM
48	48	48	IOS0
49	49	49	COM
50	50	50	OPREQ0
51	51	51	COM
52	52	52	ROW1
53	53	53	COM
54	54	54	RESET0
55	55	55	BACKI0
56	56	56	BACKO0
57	57	57	COM
58	58	58	CLOCK0
59	59	59	INTAKI0
60	60	60	INTAKO0
61	61	61	COM
62	62	62	WRP0
63	63	63	COM
64	64	64	M1IO0
65	65	65	COM
66	66	66	BREQ0
67	67	67	COM
68	68	68	PURST0
69	69	69	COM
70	70	70	OPACK1
71	71	71	COM
72	72	72	INTREQ0
73	73	73	+5 VDC
74	74	74	+5 VDC
75	75	75	+5 VDC
76	76	76	+5 VDC
77	77	77	COM
78	78	78	COM
79	79	79	COM
80	80	80	COM

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APPROVAL	DATE	BACKPLANE		
	5/25/79	DRAWING	REV	DATE
	5/25	10221	B	
			SHEET: 3	OF 3

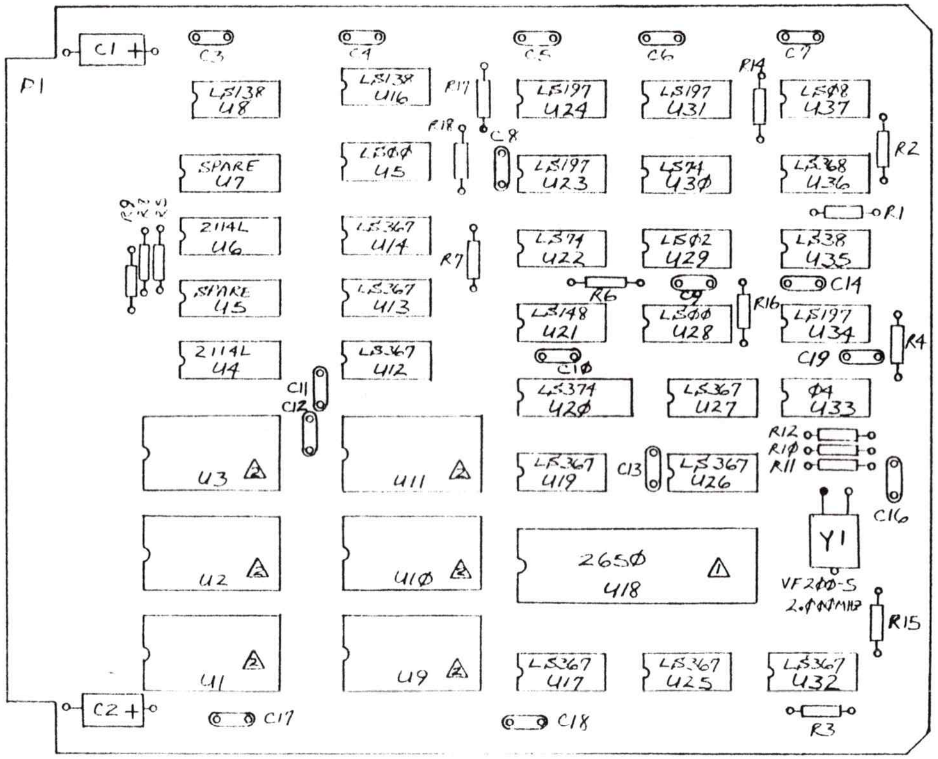
FDS-100S/9K CONTROL CIRCUIT CARD P/N 10160B

QTY	PART NUMBER	DESCRIPTION	VENDOR	REF. DESIGNATOR
1	10163	BOARD		
2	20RK022	22 MF., 25V CAP.	HOUSER	C1,C2
16	21EW010	.01 MF. CAP.	HOUSER	C3-C18
1	CM15-470J	47 PF. CAP.	HOUSER	C19
2	SN74LS00N	IC		U5,U28
1	SN74LS02N	IC		U29
1	SN7404N	IC		U33
1	SN74LS08N	IC		U37
1	SN74LS38N	IC		U35
2	SN74LS74N	IC		U30,U22
2	SN74LS138N	IC		U8,U16
1	SN74LS148N	IC		U21
4	SN74LS197N	IC		U23,U24,U31,U34
9	SN74LS367N	IC		U12,U13,U14,U17,U19,U25,U26,U27,U32
1	SN74LS368N	IC		U36
1	SN74LS374N	IC		U20
1	2650I-1	IC		U18
2	2114L	IC		U4,U6
1	VF200-5	CRYSTAL, 2.000MHZ	VALTEC	Y1
3		1.0K OHM, 1/4 W RES.		R13,R16,R18
2		1.3K OHM, 1/4 W RES.		R10,R11
8		2.0K OHM, 1/4 W RES.		R1,R2,R3,R4,R5,R14,R15,R17
1		2.4K OHM, 1/4 W RES.		R12
4		10K OHM, 1/4 W RES.		R6,R7,R8,R9
1	ICL-406-S7-G	40 PIN DIP SOCKET	R-N	U18
2	ICL-246-S7-G	24 PIN DIP SOCKET	R-N	U1,U2
REF	10161	SCHEMATIC		

G. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

APPROVAL	DATE	CONTROL CIRCUIT CARD		
KWU	5.[illegible]	DRAWING	REV	DATE
[illegible]	[illegible]	10160	B	
		SHEET: 1	OF 2	

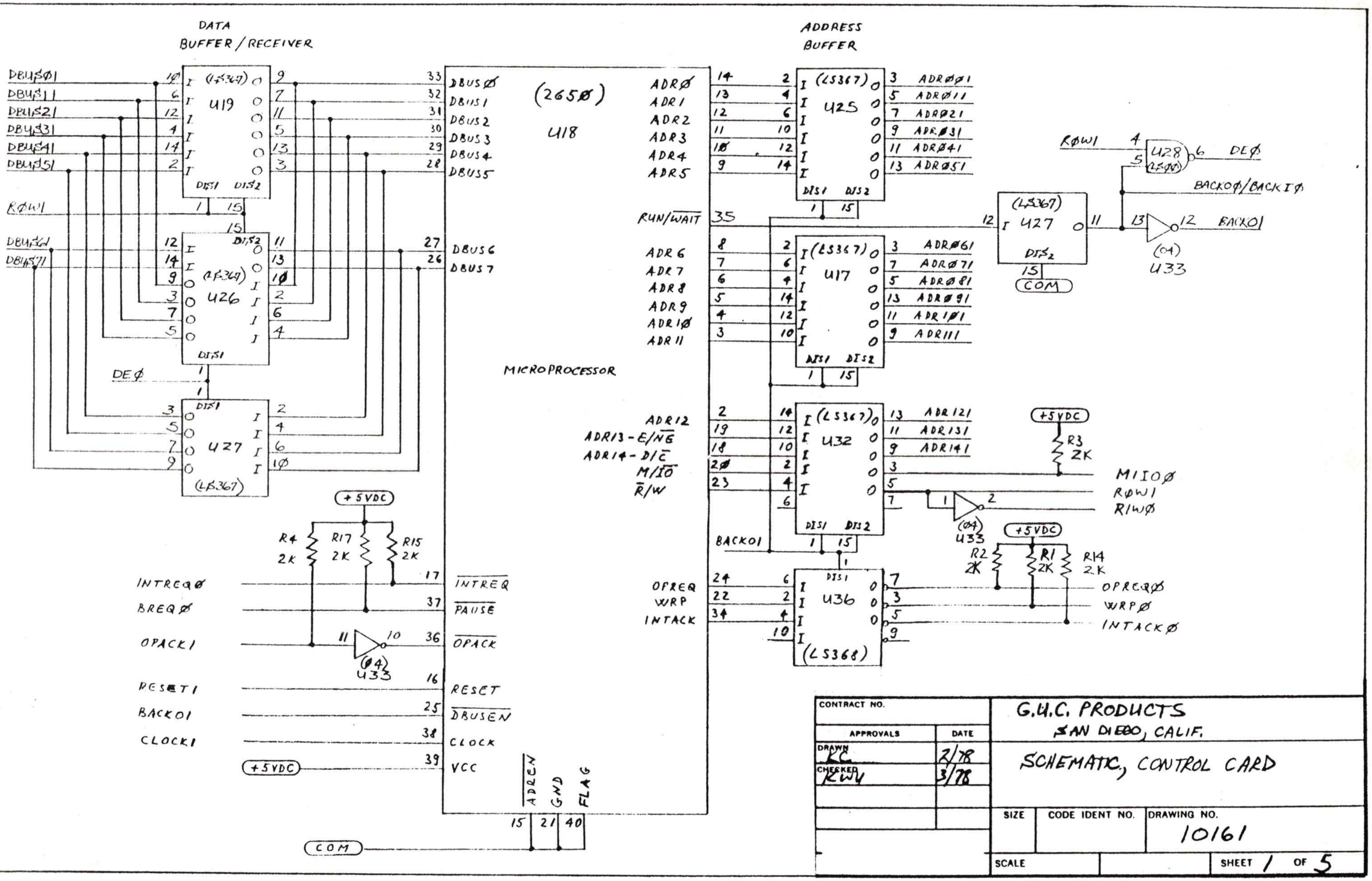
CONTROL



NOTES:

1. INSTALL SOCKET.
2. INSTALL SOCKET AND PROM AS INDICATED ON PARTS LIST.

CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	
DRAWN KWG	5/79	ASSEMBLY DRAWING, CONTROL CARD
CHECKED VB.	6/79	
SIZE	CODE IDENT NO.	DRAWING NO. 10160 REV B
SCALE		SHEET 2 OF 2



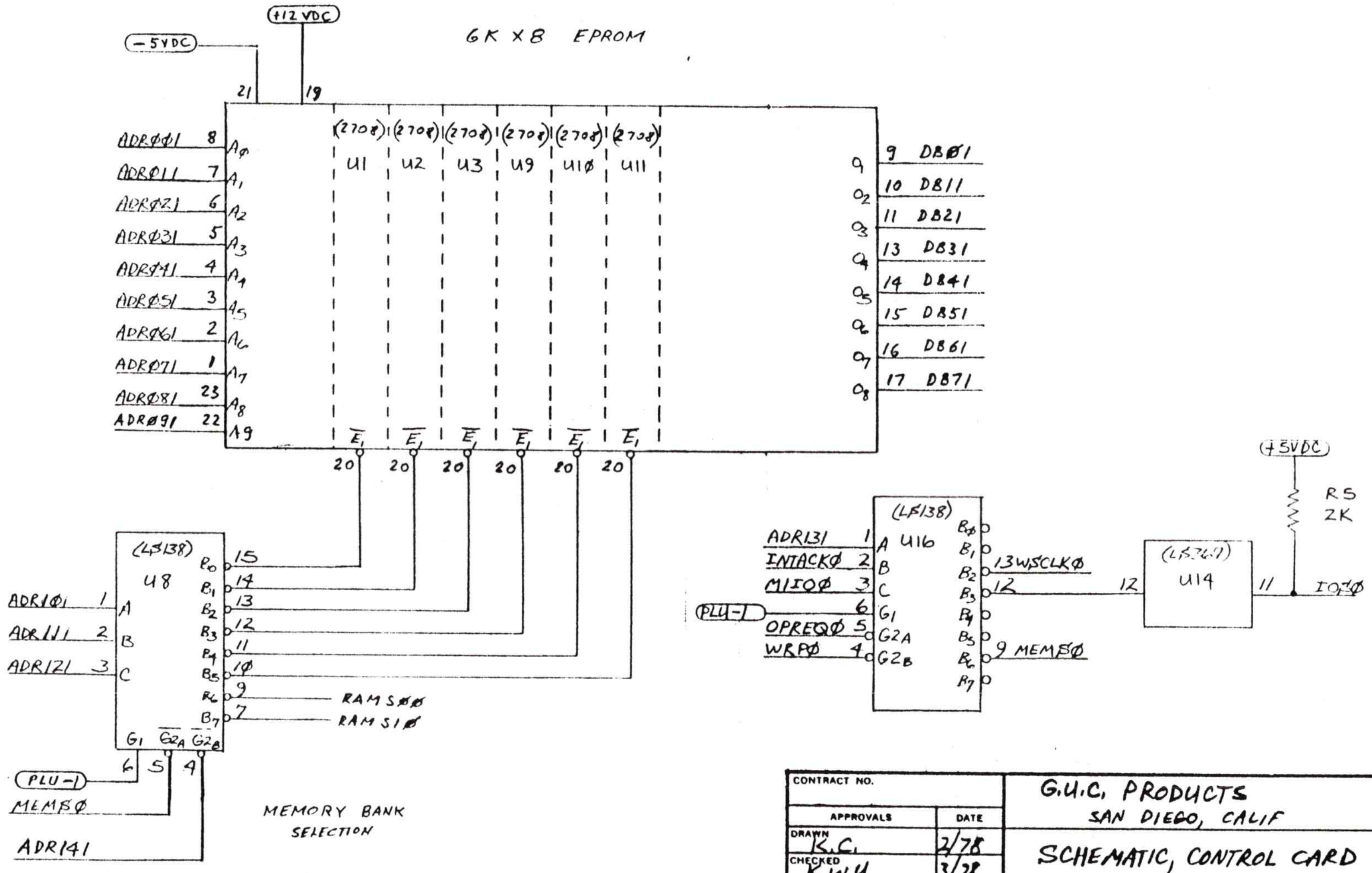
CONTRACT NO.	
APPROVALS	DATE
DRAWN KC	2/78
CHECKED RWW	3/78

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, CONTROL CARD

SIZE
CODE IDENT NO.
DRAWING NO. 10161

SCALE
SHEET 1 OF 5



CONTRACT NO.

APPROVALS | DATE

DRAWN K.C. 2/78

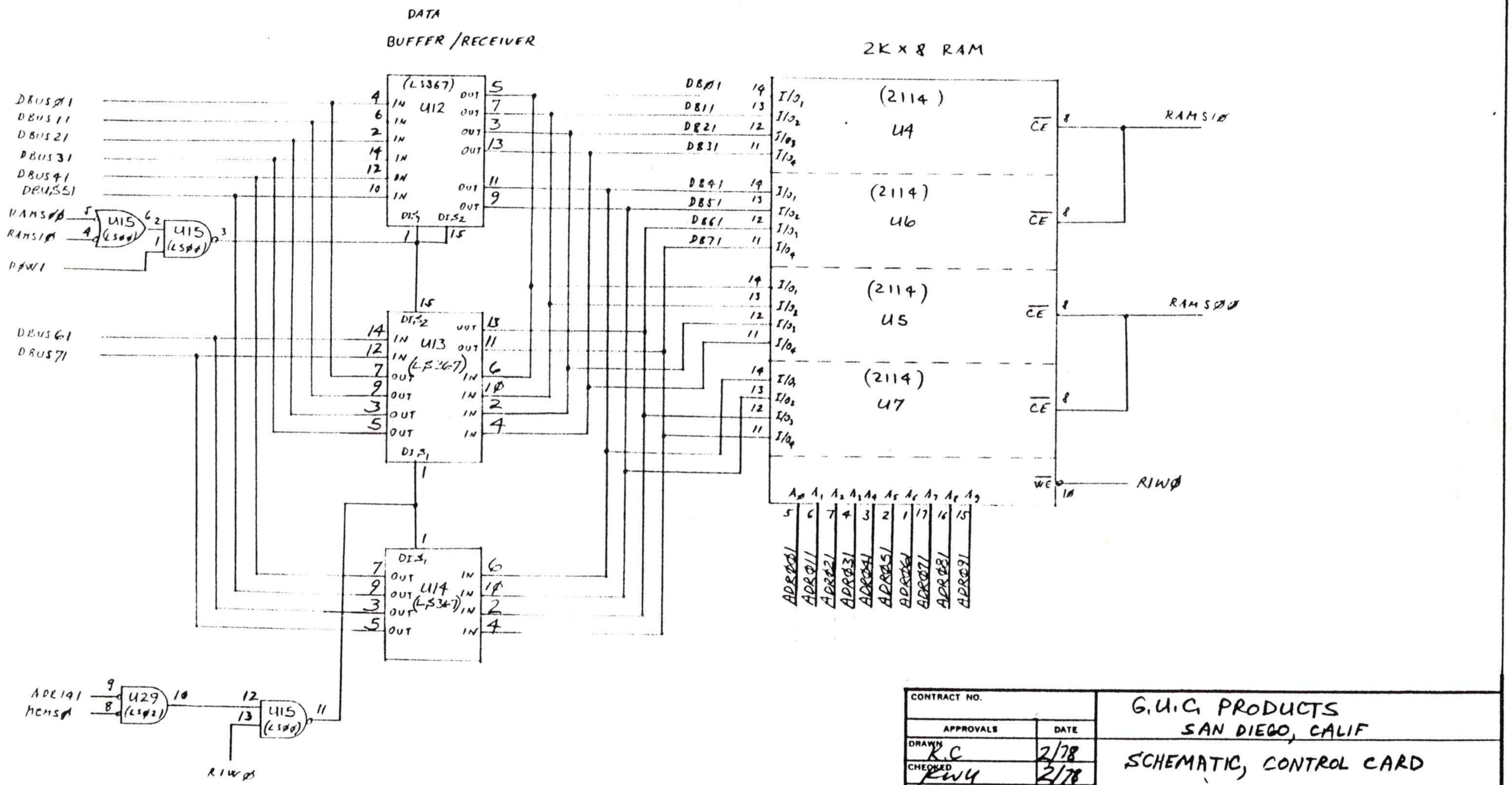
CHECKED KWH 3/78

G.U.C. PRODUCTS
SAN DIEGO, CALIF

SCHEMATIC, CONTROL CARD

SIZE
CODE IDENT NO.
DRAWING NO. 10161

SCALE
SHEET 2 OF 5



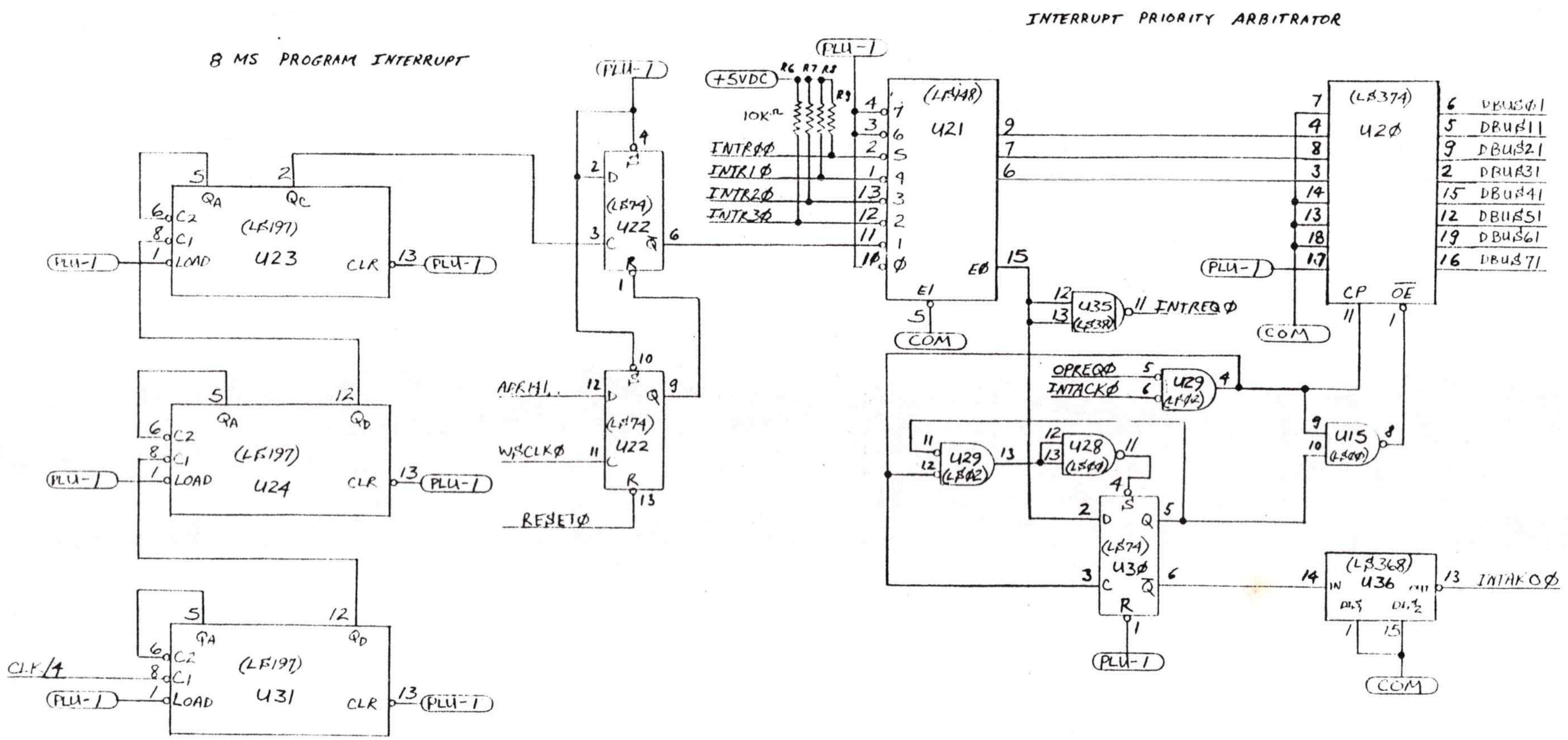
CONTRACT NO.	
APPROVALS	DATE
DRAWN K.C	2/78
CHECKED RWY	2/78

G.U.C PRODUCTS
SAN DIEGO, CALIF

SCHEMATIC, CONTROL CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10161

SCALE
SHEET 3 OF 5



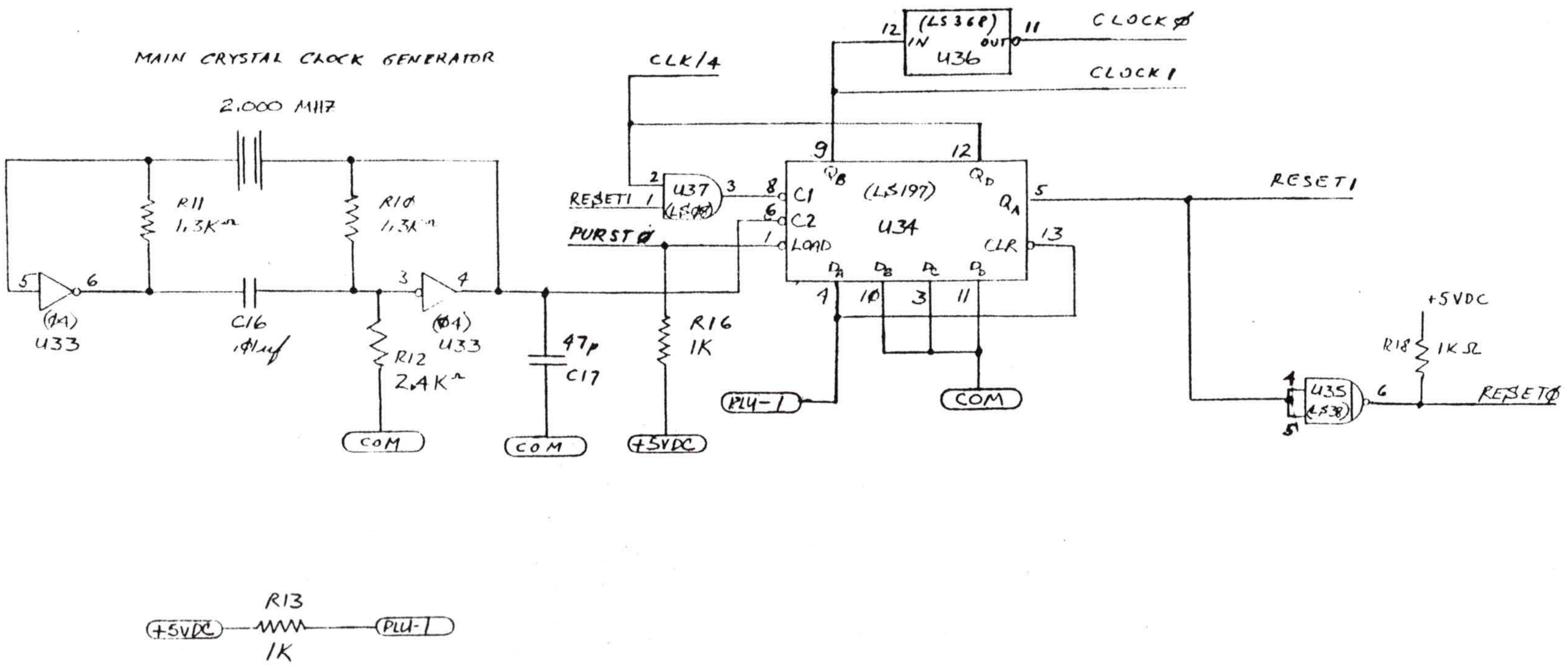
CONTRACT NO.	
APPROVALS	DATE
DRAWN KC	2/78
CHECKED KWU	2/78

GU.C. PRODUCTS
SAN DIEGO, CALIF

SCHEMATIC, CONTROL CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10161

SCALE
SHEET 4 OF 5



CONTRACT NO.	
APPROVALS	DATE
DRAWN KC	2/78
CHECKED KWK	2/78

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, CONTROL CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10161

SCALE

SHEET 5 OF 5

FDS-100S/SK DISK INTERFACE CARD P/N 10170B

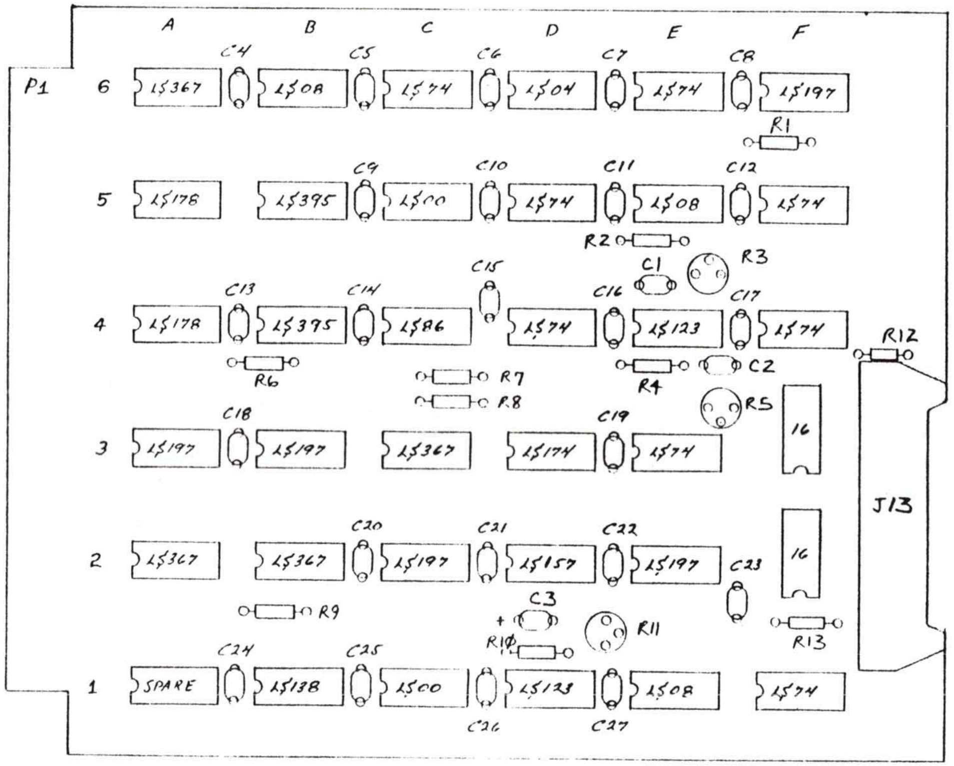
QTY	PART NUMBER	DESCRIPTION	VENDOR	REF. DESIGNATOR
1	10173	PC BOARD		
24	21EV010	.01 MF. CAP.	MOUSER	C4-C27
2	SN74LS00N	IC		1C,5C
1	SN74LS04	IC		6D
3	SN74LS08N	IC		1E,5E,6D
2	SN7416N	IC		2F,3F
8	SN74LS74N	IC		1F,3E,4D,4F,5D,5F,6C,6E
1	SN74LS86N	IC		4C
2	SN74LS123N	IC		1D,4E
1	SN74LS138N	IC		1B
1	SN74LS157N	IC		2D
1	SN74LS174N	IC		3D
2	SN74LS178N (N8270N)	IC		4A,5A
5	SN74LS197N	IC		2C,2E,3A,3B,6F
4	SN74LS367N	IC		2A,2B,3C,6A
2	SN74LS395AN	IC		4B,5B
1	3431-1002	34 PIN CONN.	3M *	J13
1	CK05BX102K	.001 MF. CAP.		C2
1	CK06BX104K	.1 MF. CAP.		C1
1	T110A105K035AS	1.0 MF. CAP.	KEMET *	C3
2	3339P-1-103	10K POT.	BOURNS	R3,R5
1	3339P-1-203	20K POT.	BOURNS	R11
7		1K OHM, 1/4 W RES.		R1,R6,R7,R8,R9,R12,R13
2		10K OHM, 1/4 W RES.		R2,R4
1		15K OHM, 1/4 W RES.		R10
REF	10171	SCHEMATIC		

* OR EQUIVALENT

S. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

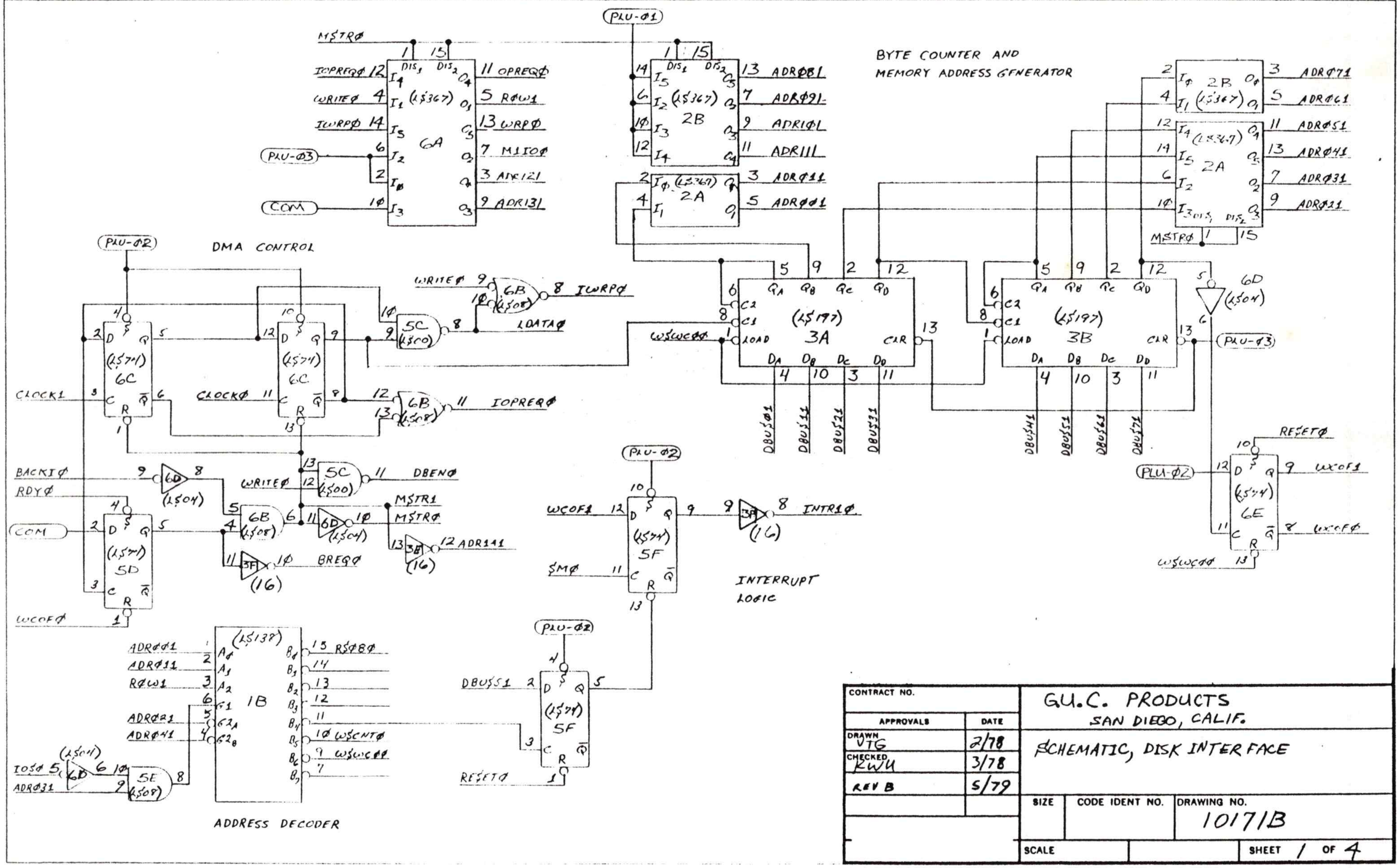
APPROVAL	DATE	DISK INTERFACE CARD		
	6/79	DRAWING	REV	DATE
	6/79	10170	B	
		SHEET: 1	OF 2	

DISK I/F



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	
DRAWN KWU	5/79	ASSEMBLY DRAWING, DISK INTERFACE CARD
CHECKED	6/79	

SIZE	CODE IDENT NO.	DRAWING NO. 10170 REV B
SCALE		SHEET 2 OF 2



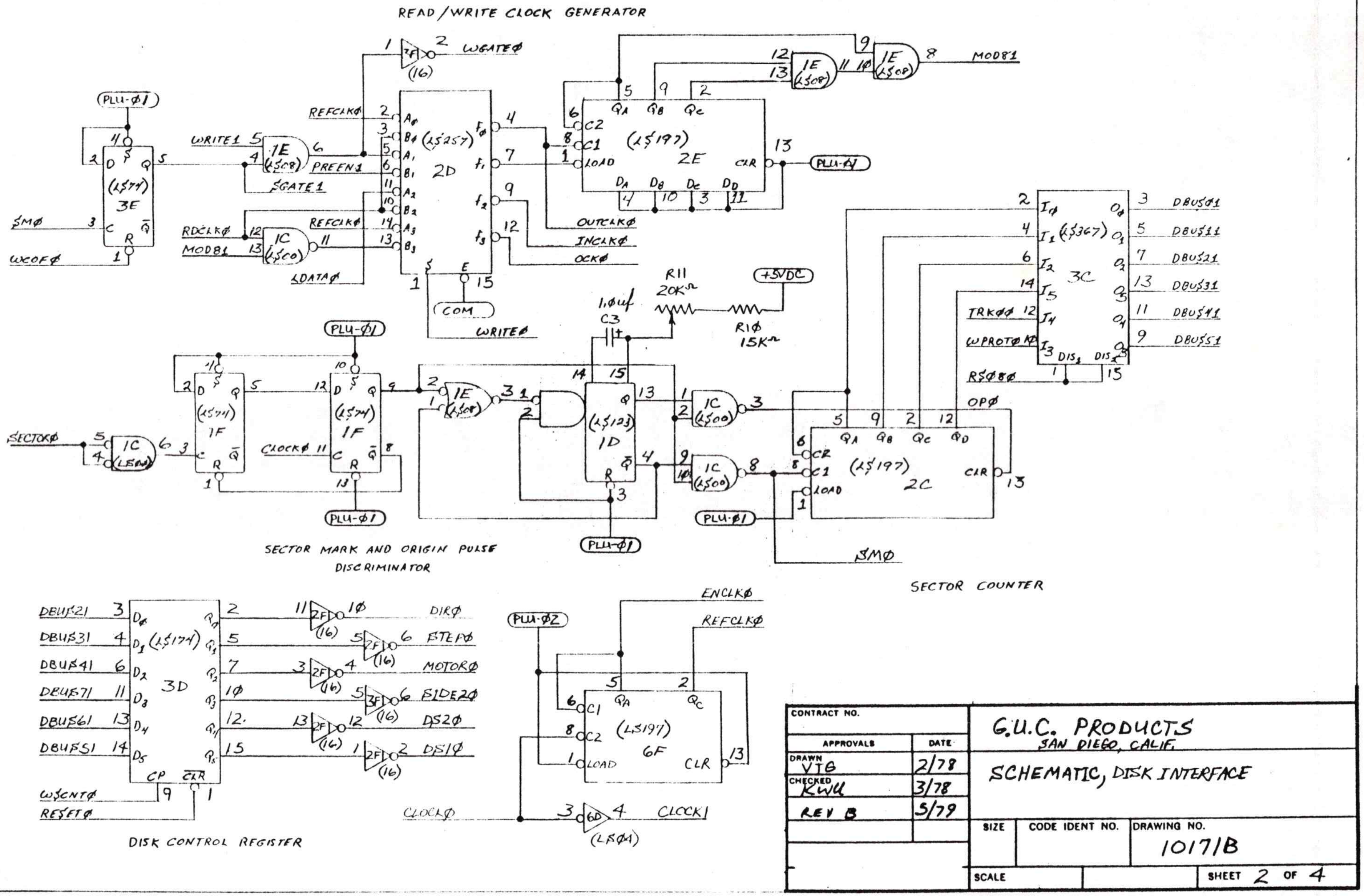
CONTRACT NO.

APPROVALS | DATE
DRAWN VTG | 2/78
CHECKED KWU | 3/78
REV B | 5/79

GU.C. PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, DISK INTERFACE

SIZE
CODE IDENT NO.
DRAWING NO. 10171B
SCALE
SHEET 1 OF 4



CONTRACT NO.

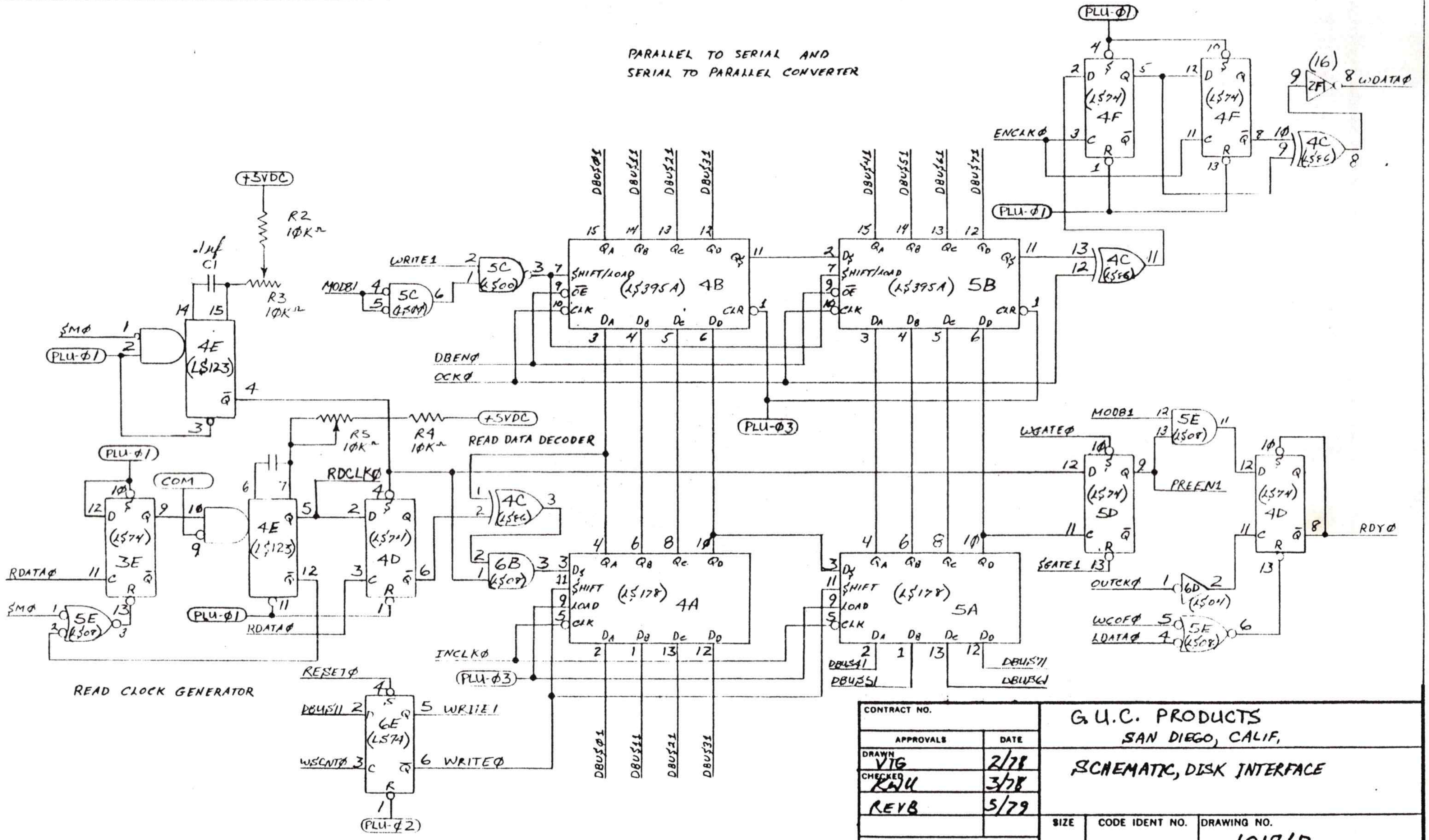
APPROVALS | DATE
DRAWN VTG 2/78
CHECKED KWU 3/78
REV B 5/79

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, DISK INTERFACE

SIZE
CODE IDENT NO.
DRAWING NO. 10171B

SCALE
SHEET 2 OF 4



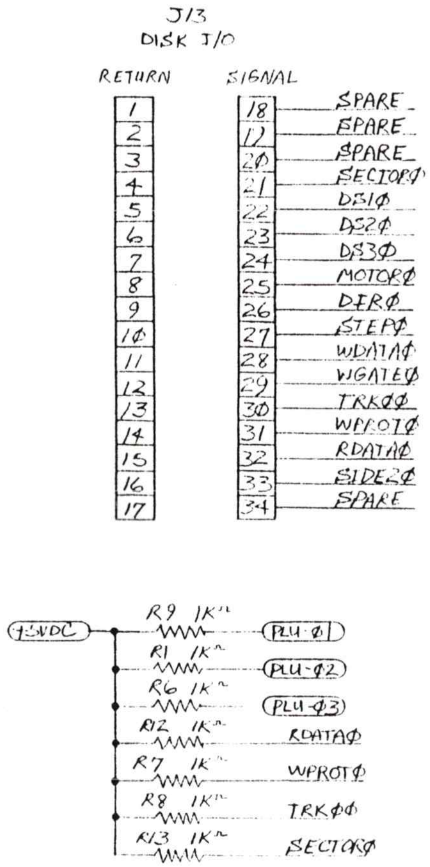
CONTRACT NO.	
APPROVALS	DATE
DRAWN VTG	2/78
CHECKED KWU	3/78
REV B	5/79

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, DISK INTERFACE

SIZE | CODE IDENT NO. | DRAWING NO. 1017/B

SCALE | SHEET 3 OF 4



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	
DRAWN		SCHEMATIC, DISK INTERFACE
CHECKED		
		SIZE · CODE IDENT NO. · DRAWING NO. 10171 B
		SCALE · SHEET 4 OF 4

P12	P13	SIGNAL
1	1	RET
2	2	RET
3	3	RET
4	4	RET
5	5	RET
6	6	RET
7	7	RET
8	8	RET
9	9	RET
10	10	RET
11	11	RET
12	12	RET
13	13	RET
14	14	RET
15	15	RET
16	16	RET
17	17	RET
18	18	SPARE
19	19	SPARE
20	20	SPARE
21	21	SECTOR0
22	22	DS10
23	23	DS20
24	24	DS30
25	25	MOTOR0
26	26	DIR0
27	27	STEP0
28	28	WDATA0
29	29	WGATE0
30	30	TRK00
31	31	WPROT0
32	32	RDATA0
33	33	SIDE20
34	34	SPARE

G. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

APPROVAL	DATE
VB	5/25/79
KWU	5/25/79

DISK I/O HARNESS

DRAWING	REV	DATE
20231	B	

SHEET: 1 OF 1

FDS-100S I/O CARD P/N 10180E

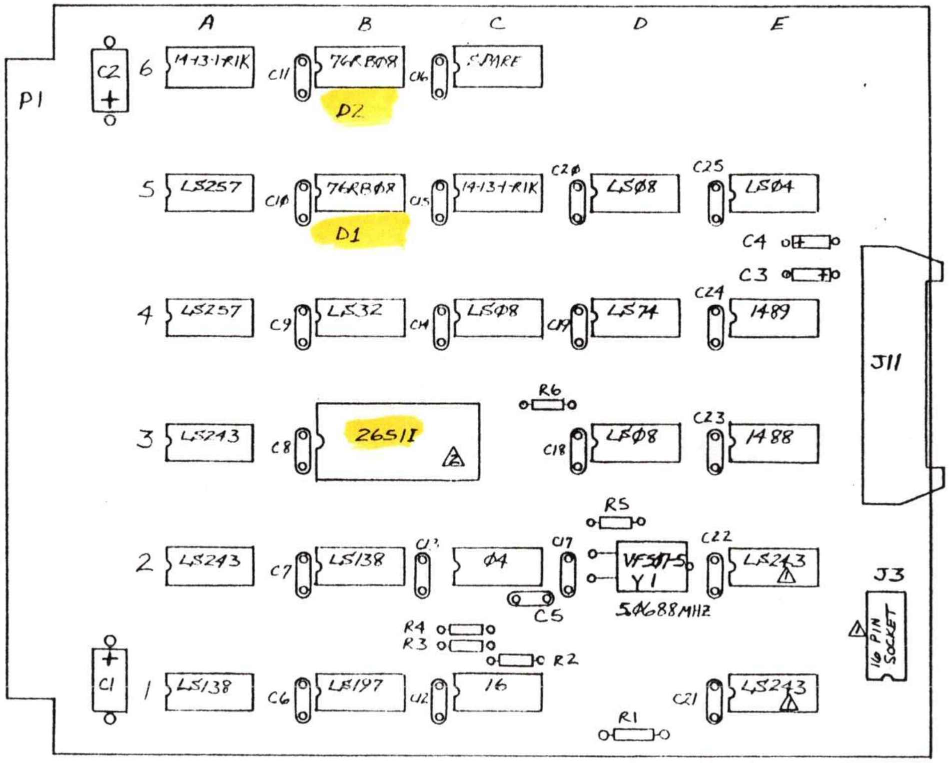
QTY	PART NUMBER	DESCRIPTION	VENDOR	REF. DESIGNATOR
1	10183	PC BOARD		
2	20RK022	22 MF., 35V CAP.	MOUSER	C1,C2
2	T110A105K035AS	1.0 MF. 35V CAP.	KEMET *	C3,C4
20	21EW010	.01 MF. CAP.	MOUSER	C6-C25
1	DM15-470J	47 PF. CAP.	MOUSER	C5
1	SN74LS04N	IC		3E
1	SN7404N	IC		2C
3	SN74LS08N	IC		3D,4C,5D
1	SN7416N	IC		1C
1	SN74LS32N	IC		4B
1	SN74LS74N	IC		4D
2	SN74LS136N	IC		1A,2B
1	SN74LS197N	IC		1B
2	SN74LS243N	IC		2A,3A
2	SN74LS257N	IC		4A,5A
1	MC1488N	IC		3E
1	MC1489N	IC		4E
1	2651I	IC		3B
1	VF507-5	CRYSTAL, 5.0688MHZ	VALTEC *	Y1
2	76RB08	DIP SWITCH	GRAYHILL *	5B,6B
3		180 OHM,1/4 W RES.		R2,R3,R4
1		220 OHM,1/4 W RES.		R5
2		10K OHM,1/4 W RES.		R1,R6
1	3429-1002	26 PIN CONN.	3M *	J11
1	ICL-163-S6-G	16 PIN DIP SOCKET	R-N	J3
1	ICL-286-S7-G	28 PIN DIP SOCKET	R-N	3B
REF	10181	SCHEMATIC		

* OR EQUIVALENT

G. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

APPROVAL	DATE	SERIAL I/O CARD		
KWI	5/79	DRAWING	REV	DATE
VS	6/79	10180	E	
		SHEET: 1	OF 2	

SERIAL I/O



NOTES:

- △1 INSTALL ONLY FOR -1 CONFIGURATION.
- △2 SOCKET INSTALLED.

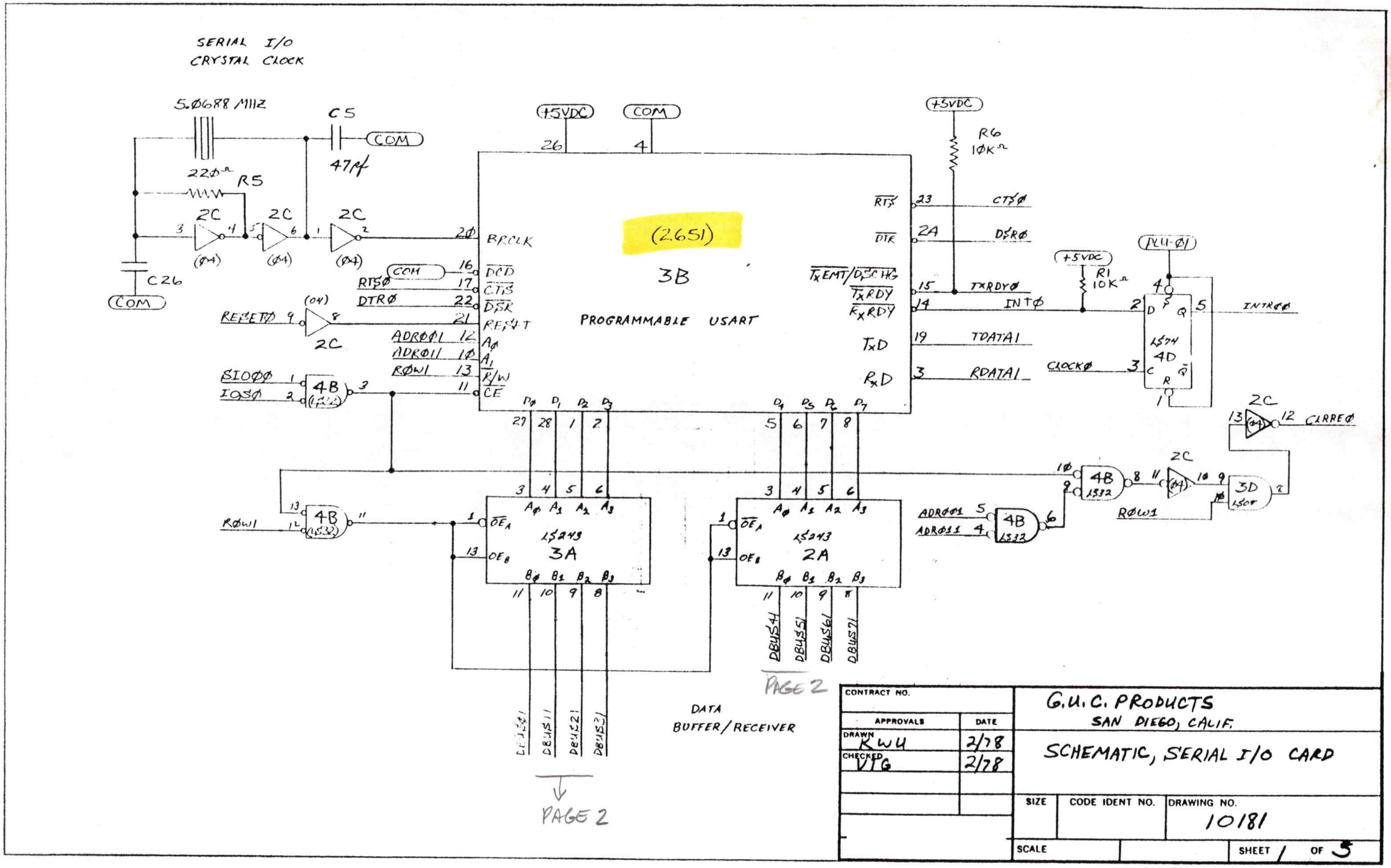
CONTRACT NO.	
APPROVALS	DATE
DRAWN KWU	5/79
CHECKED	6/79

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

ASSEMBLY DRAWING, SERIAL I/O CARD

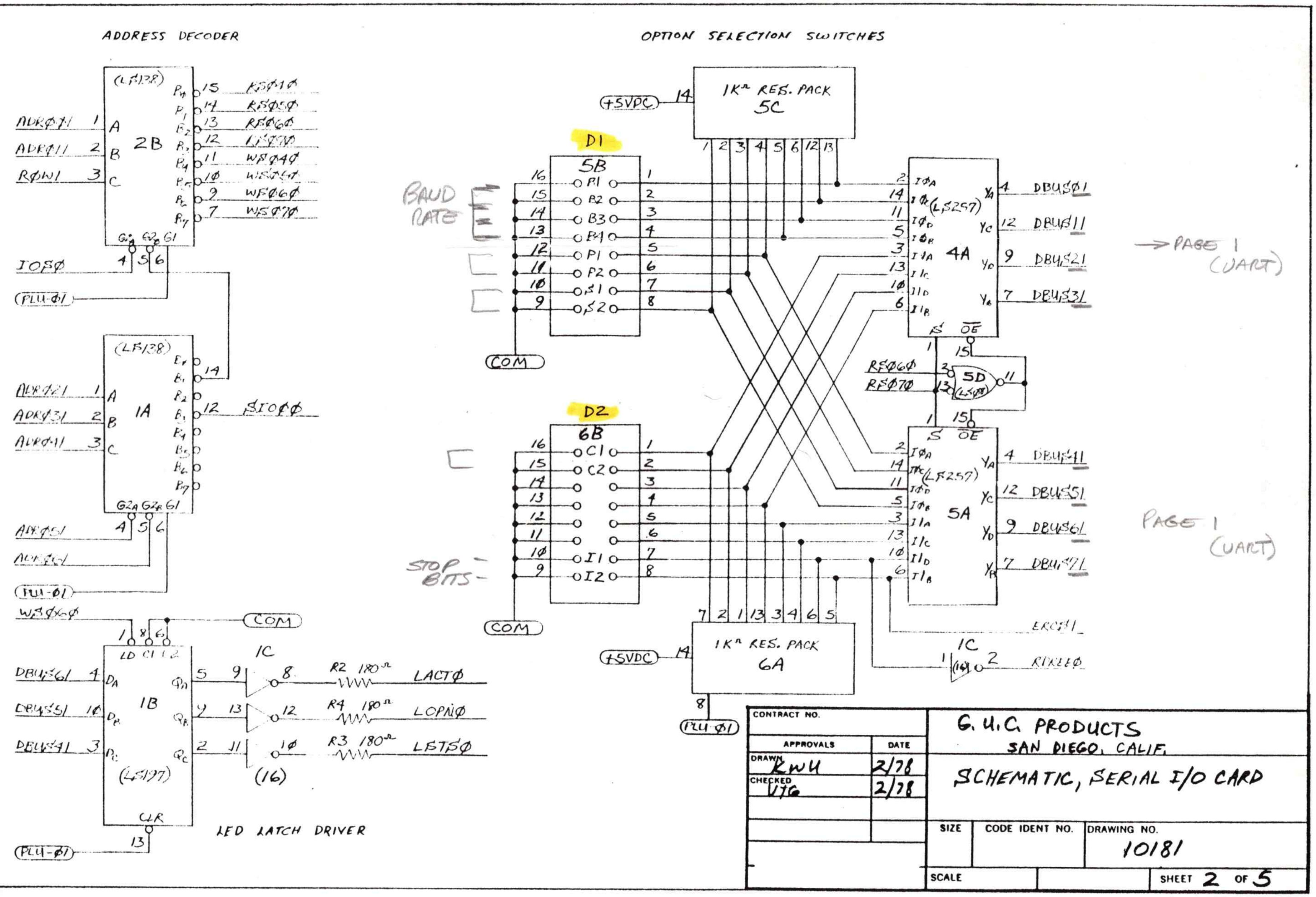
SIZE	CODE IDENT NO.	DRAWING NO.
		10180 REV E

SCALE
SHEET 2 OF 2



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	SCHEMATIC, SERIAL I/O CARD
DRAWN KWU	2/78	
CHECKED VTG	2/78	

SIZE	CODE IDENT NO.	DRAWING NO. 10181
SCALE		SHEET 1 OF 5



CONTRACT NO.	
APPROVALS	DATE
DRAWN KWH	2/78
CHECKED VTG	2/78

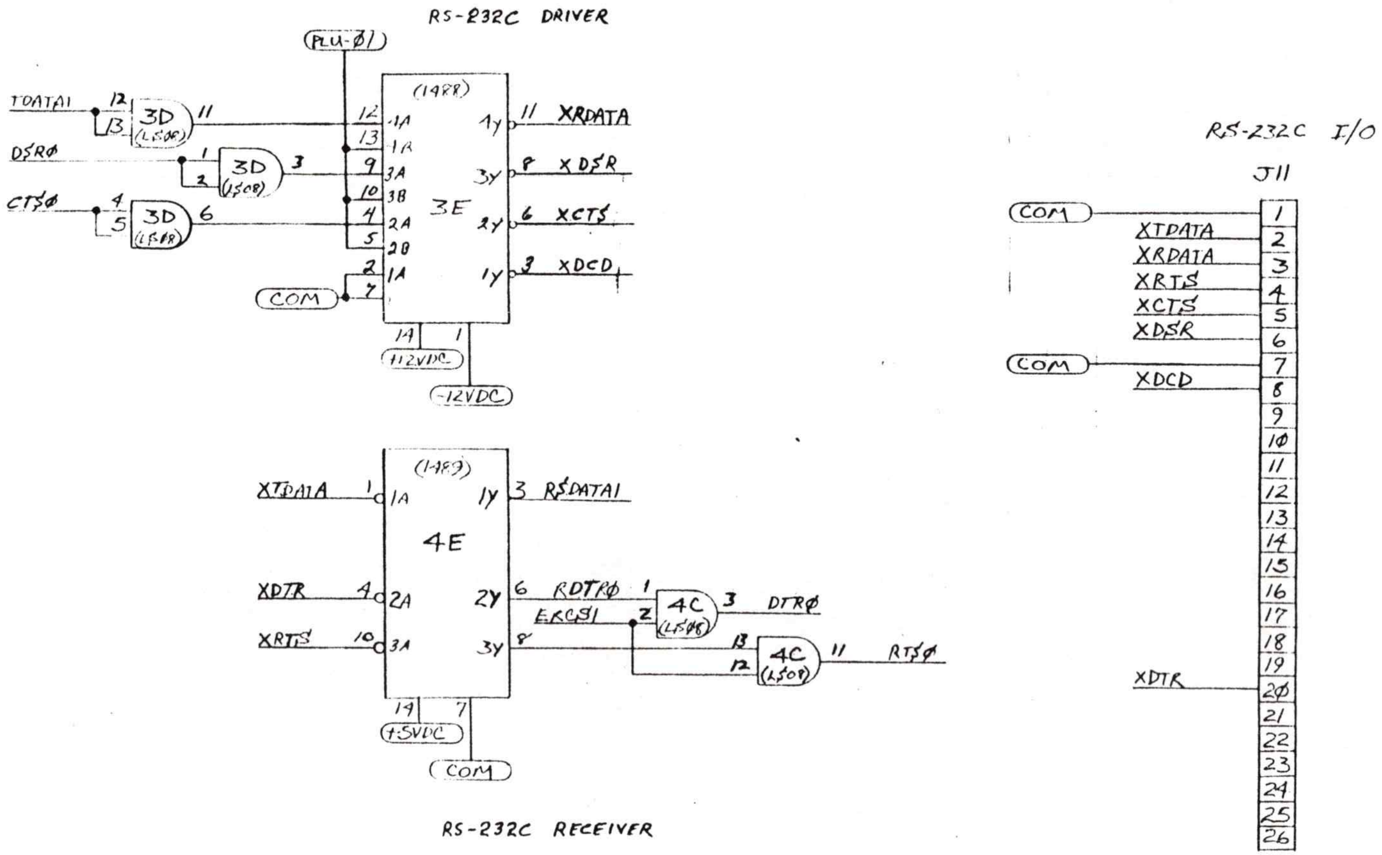
G.U.C PRODUCTS
SAN DIEGO, CALIF.

SCHEMATIC, SERIAL I/O CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10181

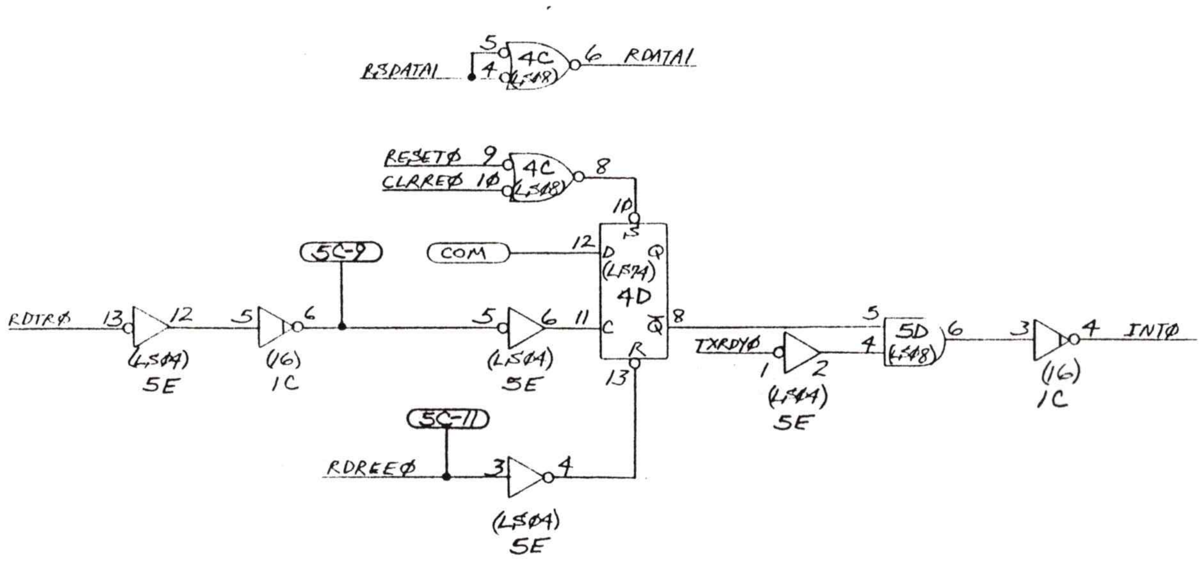
SCALE

SHEET 2 OF 5



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	
DRAWN KWU	2/78	SCHEMATIC, SERIAL I/O CARD
CHECKED VTG	2/78	

SIZE	CODE IDENT NO.	DRAWING NO. 10181
SCALE		SHEET 3 OF 5



READ ENABLE LOGIC

CONTRACT NO.	
APPROVALS	DATE
DRAWN KWH	2/78
CHECKED VTG	2/78

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

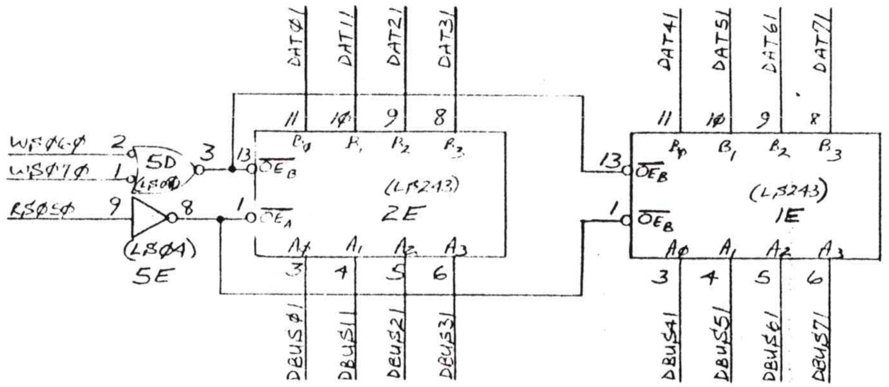
SCHEMATIC, SERIAL I/O CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10181

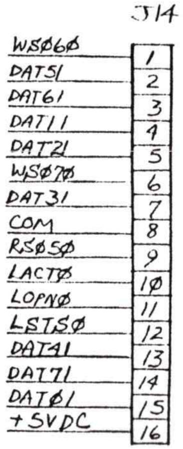
SCALE

SHEET 4 OF 5

KEYBOARD BUFFER/RECEIVER



KEYBOARD/DISPLAY I/O



CONTRACT NO.

APPROVALS	DATE
DRAWN KWH	2/78
CHECKED VTG	2/78

G.U.C. PRODUCTS
SAN DIEGO, CALIF.

SCEMATIC, SERIAL I/O CARD

SIZE
CODE IDENT NO.
DRAWING NO. 10181
SCALE
SHEET 5 OF 5

J10		P11	INTERFACE SIGNAL		ASSIGNMENT
1	<-->	1	PROTECTIVE GROUND	*	COM
2	--->	2	TRANSMITTED DATA	*	XTDATA
3	<---	3	RECEIVED DATA	*	XRDATA
4	--->	4	REQUEST TO SEND	*	XRTS
5	<---	5	CLEAR TO SEND	*	XCTS
6	<---	6	DATA SET READY	*	XDSR
7	<-->	7	SIGNAL GROUND	*	COM
8	<---	8	RECEIVED LINE SIGNAL DETECTOR	*	XDCD
9		9	RESERVED	*	NOT USED
10		10	RESERVED	*	NOT USED
11		11	UNASSIGNED	*	NOT USED
12		12	SEC. REC'D LINE SIG. DETECTOR	*	NOT USED
13		13	SEC. CLEAR TO SEND	*	NOT USED
14		14	SECONDARY TRANSMITTED DATA	*	NOT USED
15		15	TRANSMISSION SIGNAL ELEMENT TIMING	*	NOT USED
16		16	SECONDARY RECEIVED DATA	*	NOT USED
17		17	RECEIVER SIGNAL ELEMENT TIMING	*	NOT USED
18		18	UNASSIGNED	*	NOT USED
19		19	SECONDARY REQUEST TO SEND	*	NOT USED
20	--->	20	DATA TERMINAL READY	*	XDTR
21		21	SIGNAL QUALITY DETECTOR	*	NOT USED
22		22	RING INDICATOR	*	NOT USED
23		23	DATA SIGNAL SELECTOR	*	NOT USED
24		24	TRANSMIT SIGNAL ELEMENT TIMING	*	NOT USED
25		25	UNASSIGNED	*	NOT USED

G. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

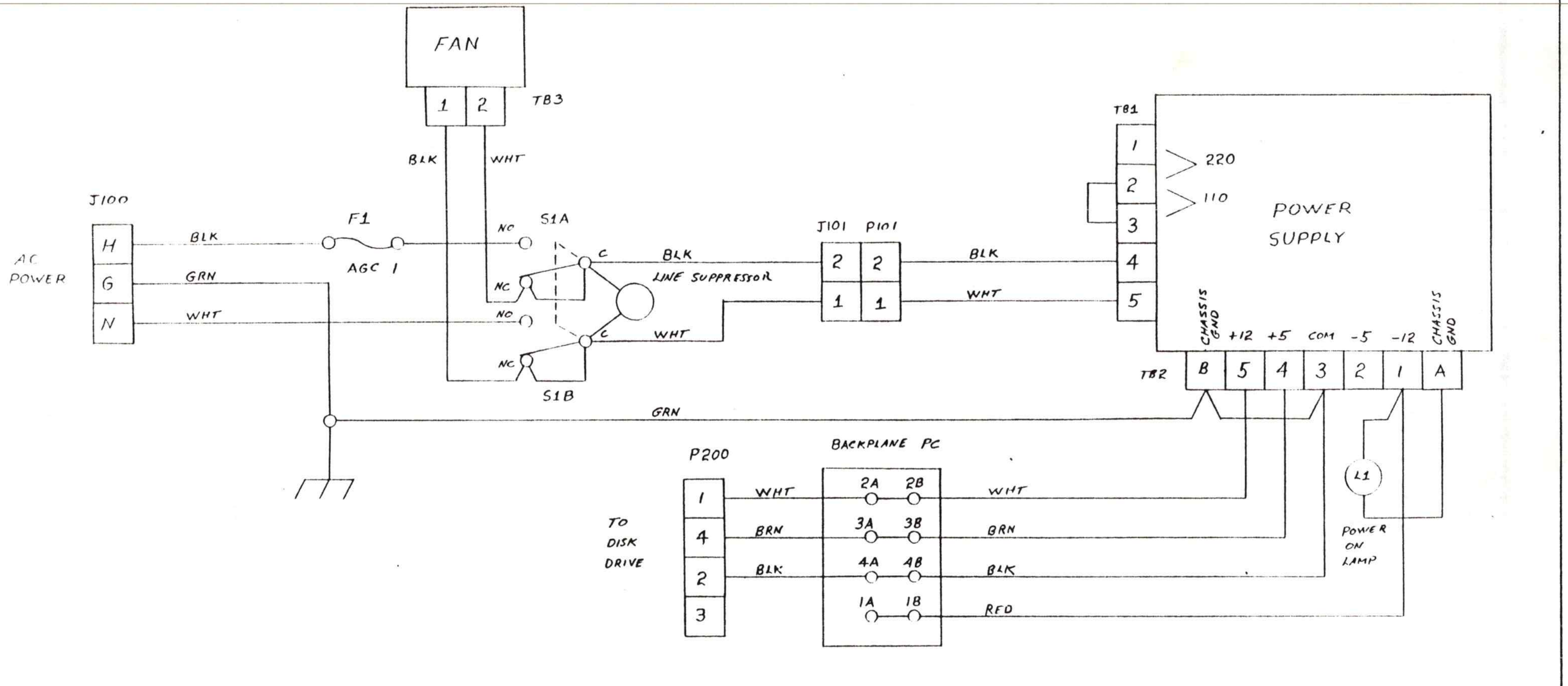
APPROVAL	DATE	SERIAL I O HARNESS		
	5/25/79	DRAWING	REV	DATE
	5/25/79	20241	B	
		SHEET: 1 OF 1		

FDS-100S REAR PANEL ASSEMBLY P/N 10060

QTY	PART NUMBER	DESCRIPTION	VENDOR
1	20150	REAR PANEL	
1	EAC-302	POWER CORD CONNECTOR	SWITCHCRAFT *
1	LE21A	POWER SWITCH	RAYTHEON *
1	504-4405	FUSE BLOCK	MOUSER
1	760 99XW 182 11115	FAN	ETRI *
1	V130LA10A	VARISTOR	GE
1	20280	FAN GUARD	
1	20240	I/O HARNESS	
1	1-480318-0	HOUSING	AMP
1	1-480319-0	HOUSING	AMP
2	60619-1	CRIMP SOCKETS	AMP
2	60620-1	CRIMP PINS	AMP
2		20 GA., #6 RING TERMINALS	
3		1/8X1/4 POP RIVETS	
3		6-32X5/8 PAN HD PHLPS SCREW	
1		6-32X5/16 PAN HD PHLPS SCREW	
4		#6 NUT	
12		#6 FLAT WASHER	
2		4-40X1/2 PAN HD PHLPS SCREW	
2		4-40 NUT	
2		#4 FLAT WASHER	
2		#4 LOCK WACHER	

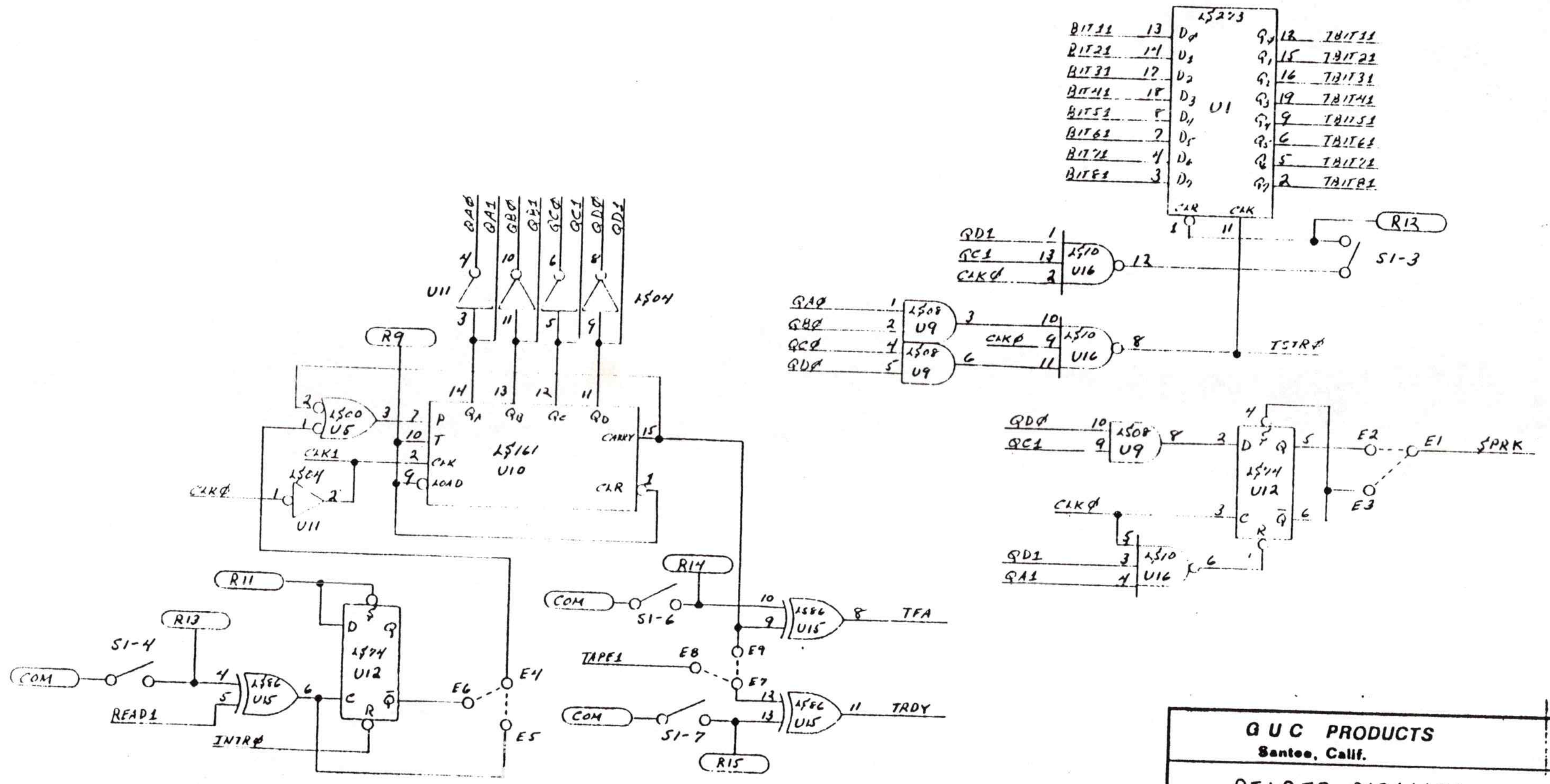
G. U. C. PRODUCTS
SAN DIEGO, CALIFORNIA

APPROVAL	DATE	REAR PANEL ASSEMBLY		
	5/22			
	5/29	DRAWING	REV	DATE
		10060	A	
		SHEET: 1	OF 1	



CONTRACT NO.		G.U.C. PRODUCTS SAN DIEGO, CALIF.
APPROVALS	DATE	SCHEMATIC, POWER DISTRIBUTION
DRAWN J.B.	5/79	
CHECKED Kull	5/79	

SIZE	CODE IDENT NO.	DRAWING NO. 10231
SCALE		SHEET 1 OF 1

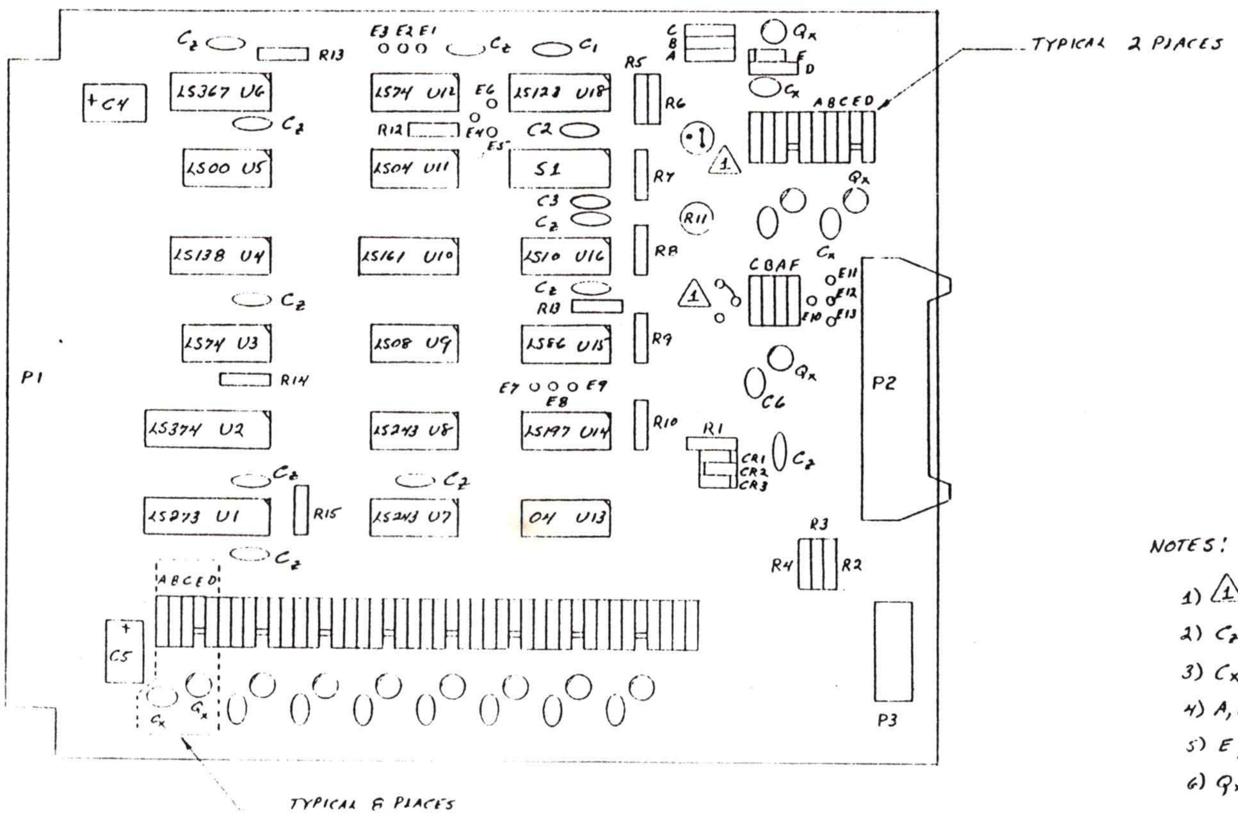


QUC PRODUCTS
Santee, Calif.

READER PARALLEL
INTERFACE

SIZE	CODE IDENT NO.	DRAWING NO.
		10191

SCALE | SHEET 1 OF 3



NOTES: UNLESS OTHERWISE SPECIFIED

1) $\triangle$1 INSTALL JUMPER, TYP 2 PLACES
2) C_z CAP, TYP 12 PLACES
3) C_x CAP, TYP 11 PLACES
4) A, B, C, D – RESISTOR, TYP 11 PLACES
5) E, DIODE, TYP 11 PLACES
6) Q_x, TRANSISTOR, TYP 11 PLACES

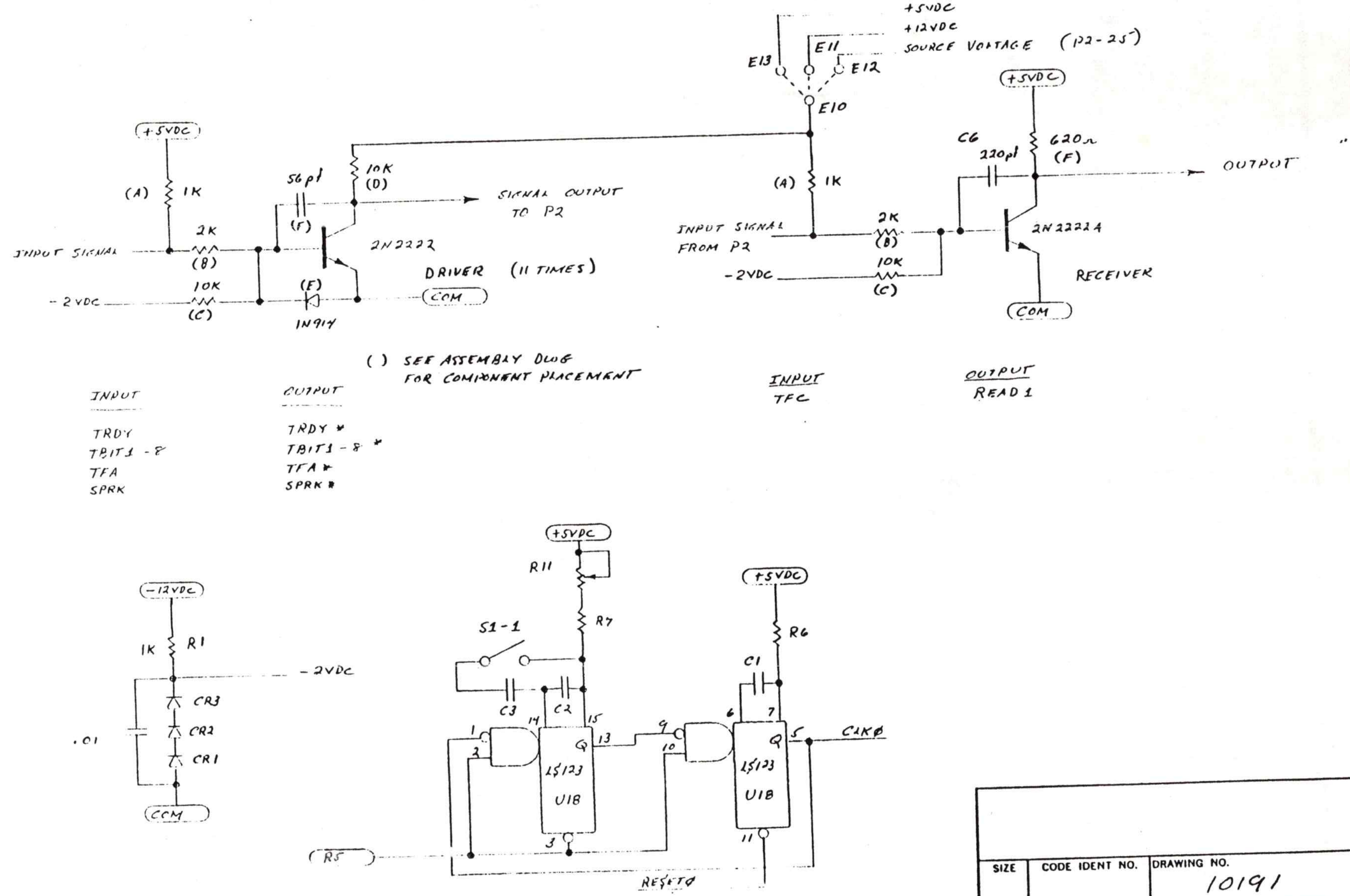
CONTRACT NO.		
APPROVALS		DATE
DRAWN	V.S.	8/81
CHECKED		8/81

G.U.C. Products
Santee, Calif.

ASSEMBLY DRAWING,
PARALLEL I/O CARD

SIZE	CODE IDENT NO.	DRAWING NO.
		10190

SCALE | REV B | SHEET 2 OF 2

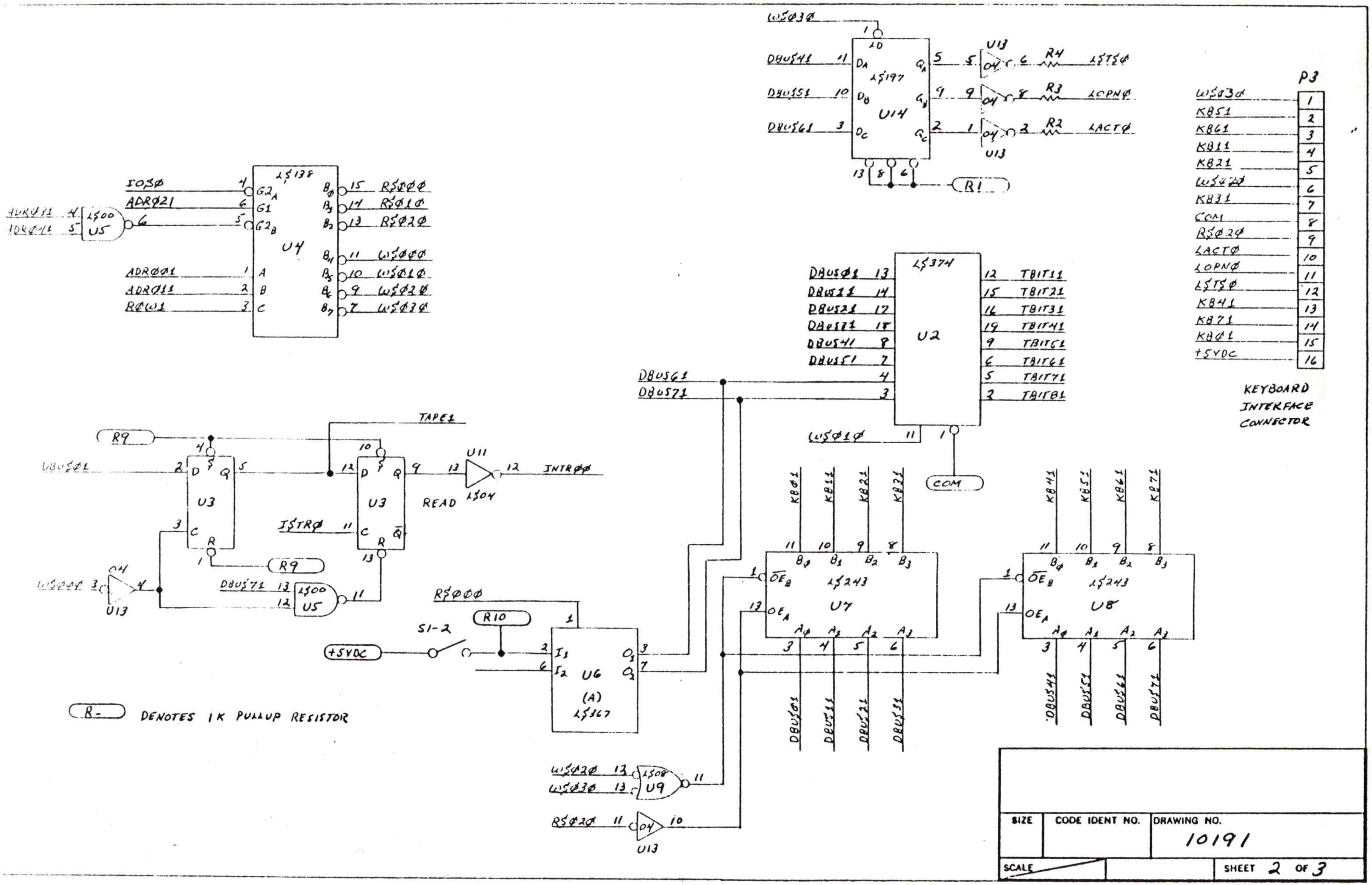


( ) SEE ASSEMBLY DWG FOR COMPONENT PLACEMENT

INPUT	OUTPUT
TRDY	TRDY *
TBIT1 - 8	TBIT1 - 8 *
TFA	TFA *
SPRK	SPRK *

INPUT	OUTPUT
TFC	READ 1

SIZE	CODE IDENT NO.	DRAWING NO. 10191
SCALE		SHEET 3 OF 3



SIZE	CODE IDENT NO.	DRAWING NO.
		10191

SCALE

SHEET 2 OF 3